WT56F248/232
1T 8052 Micro-controller with ADC + LCD Driver (FLASH)

Data Sheet

Rev. 1.02

September 2022

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1. General Description

The WT56F248/232 is a general-purpose single chip Microcontroller with LCD function provided by Weltrend, a well-known IC Design House in Taiwan. In addition to using the advanced IT 8052 single-chip core, wide and low operating voltage range (2.2V ~ 5.5V), and high noise immunity, the product consists of 48Kx8 (32Kx8 for WT56F232) Flash Program Memory, 1024x8 RAM (768x8 for WT56F232), abundant peripheral resources and versatile power management (refer to the content for more details).

The above features make the WT56F248/232 suitable for a wide range of applications, especially in areas such as home appliances with LCD (rice cooker, microwave oven, and toaster), Thermo-Hygrometer, bidirectional car alarm, remote controller of air conditioner, and so on.

The WT56F248/232 is a low cost high performance product with kinds of package to replace the mainstream products on the market (refer to “Pin Configuration” section for more details). In order to contribute more competitive ability, Weltrend also provides dice and wafer sale for the customer.

Part No.	PROM (Byte)	SRAM (Byte)	I/O (Max)	LCD (SxC)	PWM (BitxCh)	ADC (BitxCh)	PKG Type
WT56F216	16K	384	44	8(4)x19 8(4)x16(20)	16-bitx2	12-bitx16	44LQFP 28SOP
WT56F232	32K	768	54	8(4)x19 8(4)x16(20)	16-bitx6	12-bitx16	64LQFP 44LQFP 32QFN
WT56F248	48K	1024	54	8(4)x19 8(4)x16(20)	16-bitx6	12-bitx16	64LQFP 44LQFP 32QFN

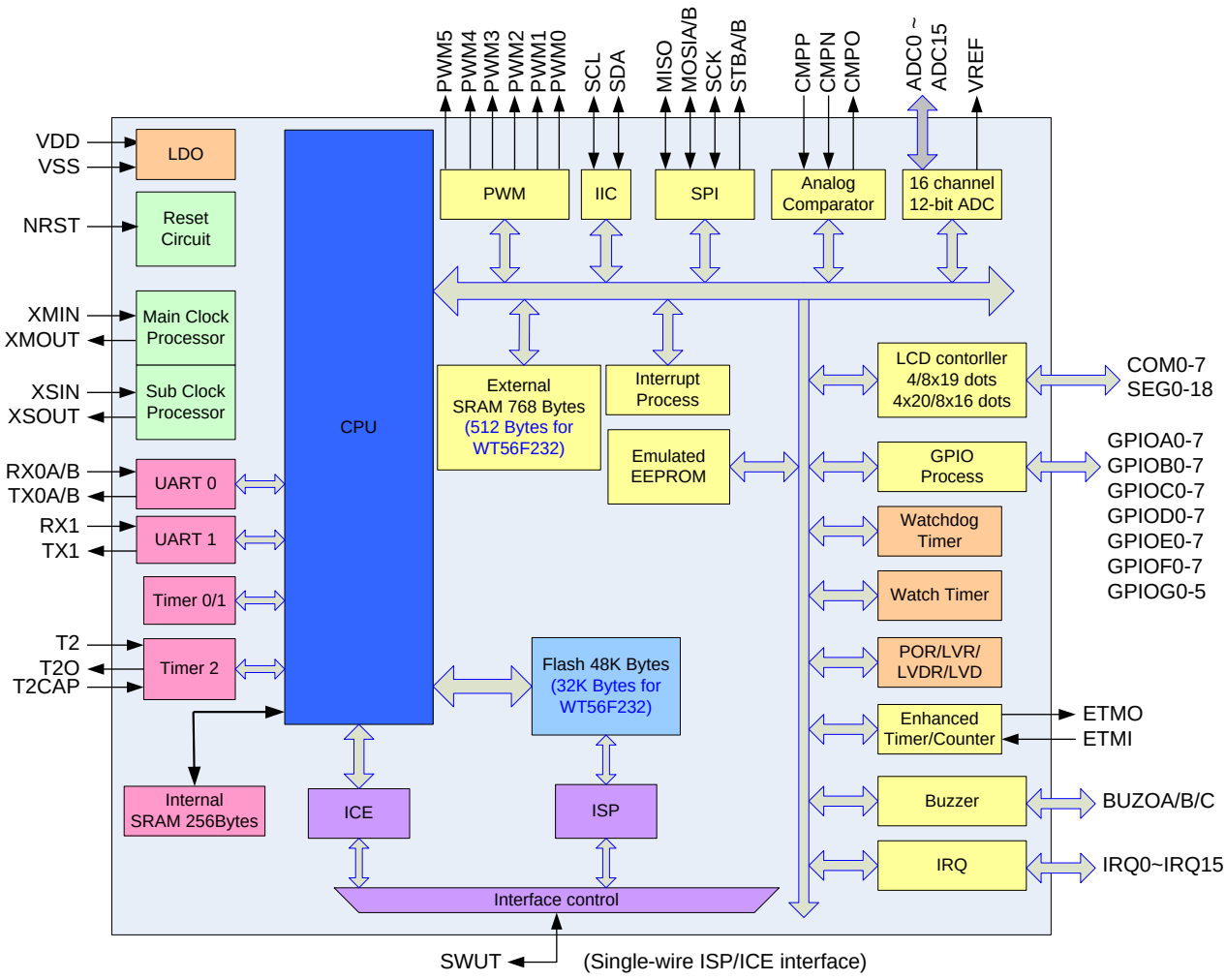
2. Features

WT56F248/232 is an advanced 8052 Micro-controller with LCD Driver, and it also provides the following features.

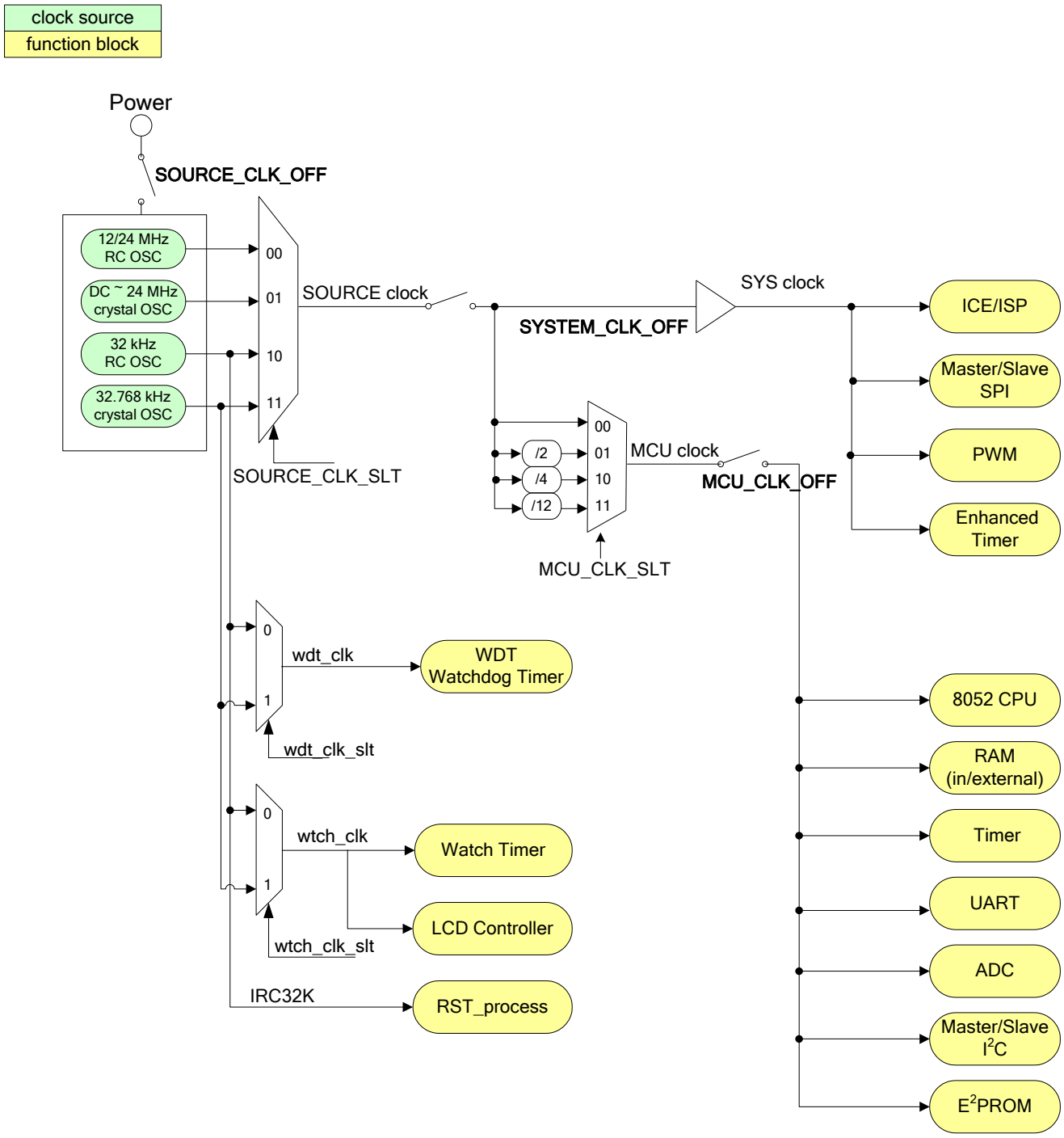
- 1T 8052 core, MCS-51 instruction set compatible
- Instruction execution time: Min. = 41.67ns @24 MHz
- 1024/768 Bytes of RAM (256 Bytes of standard 8052 internal Data RAM and 768/512 Bytes of external RAM)
- 48K Bytes of flash memory for program storage (32K Bytes for WT56F232)
- Supporting Dual Clock Oscillators:
  - Main clock: External DC ~ 24 MHz Crystal Oscillator or Internal 12/24 MHz RC
  - Sub clock: External 32.768 kHz Crystal Oscillator or Internal 32 kHz RC
- Dual 16-bit Data Pointers (DPTR0 & DPTR1)
- Three 16-bit Timer/Counters (Timer0, Timer1, Timer2)
- One Watchdog Timer (WDT)
- One Watch Timer
- One 16-bit Enhanced Timer with Capture function
- Two UARTs (UART0, UART1), support baud rate 1200 bps ~ 230400 bps (at 24 MHz)
- Emulated E^2PROM

- One master/slave SPI interface
- One master/slave I^2C interface
- Six 16-bit PWMs (PWM0~5)
- LCD Control Driver
  - Mode A: 4 COM x 19 SEG or 8 COM x 19 SEG
  - Mode B: 4 COM x 20 SEG or 8 COM x 16 SEG
- 16-channel 12-bit Analog/Digital Converter (ADC0 ~ ADC15) with Voltage Reference source
- One Comparator with 32-level Voltage Reference sources
- Three power-saving modes: Sleep mode, Green mode and Idle mode
- 16 external Interrupt IRQ pins (IRQ0 ~ IRQ15)
- 54 programmable bi-directional I/O pins, 15 of them with both high current sink/source ability (20 mA)
- One Buzzer, with four selectable frequencies and three output paths
- Low Voltage Detection (LVD) and Low Voltage Detection Reset (LVDR), both of them are programmable
- On-chip Power On Reset (POR) and Low Voltage Reset (LVR)
- Built-in single-wire In-Circuit Emulator (ICE) and In-System Program (ISP)
- Read Out Protection and Code Encryption
- Operating voltage range: 2.2V ~ 5.5V
- Operating temperature: -40℃ ~ +105℃
- Green Package: LQFP64, LQFP44, and QFN32

3. Block Diagram



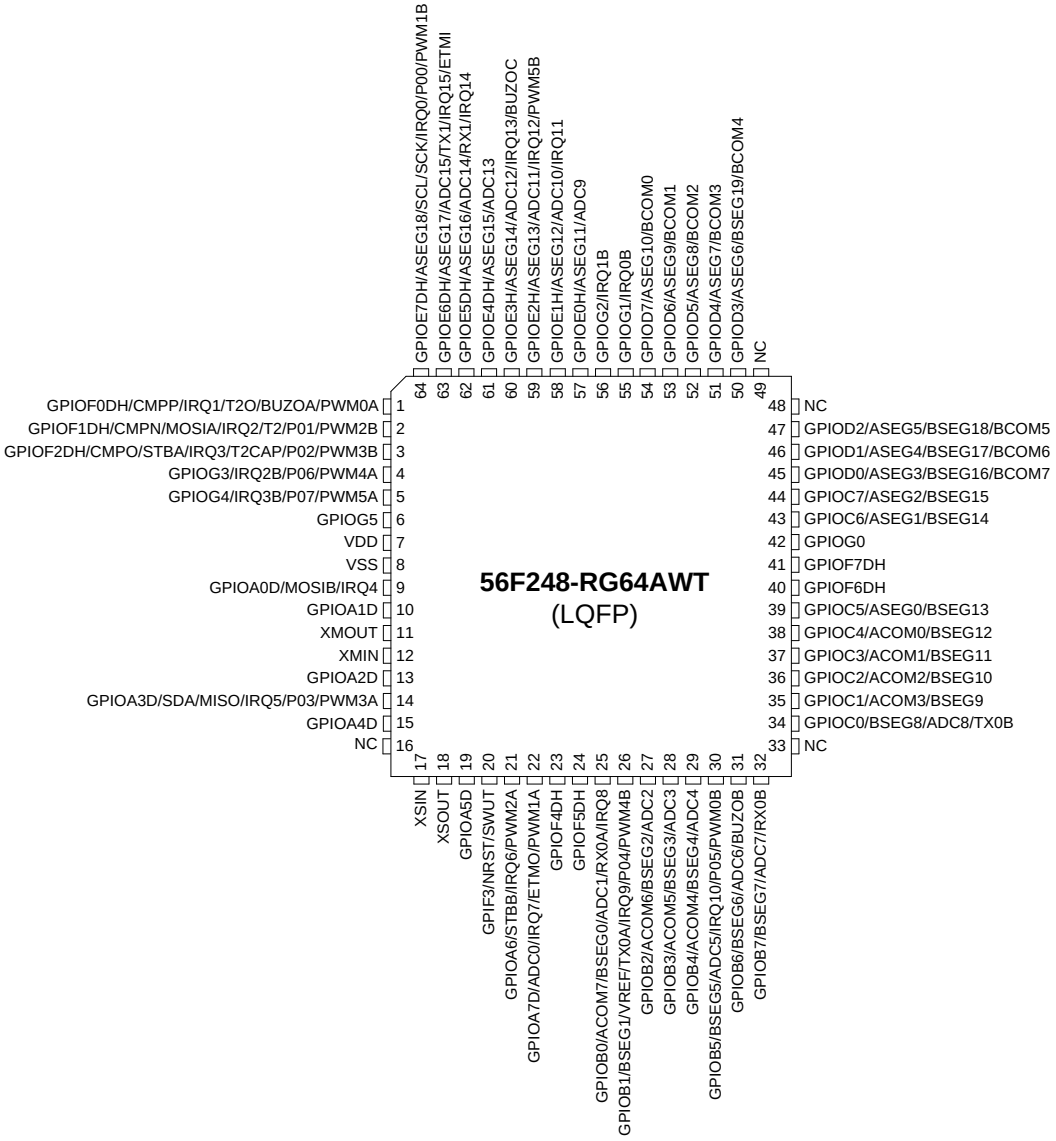
3.1 System Clock Tree



* When using the external Crystal Oscillator, please select the corresponding driving ability according to its frequency. Refer to Oscillator Driver Control Register (XFR: 0x08) CRY_12M_DR[1:0] bit for more details.

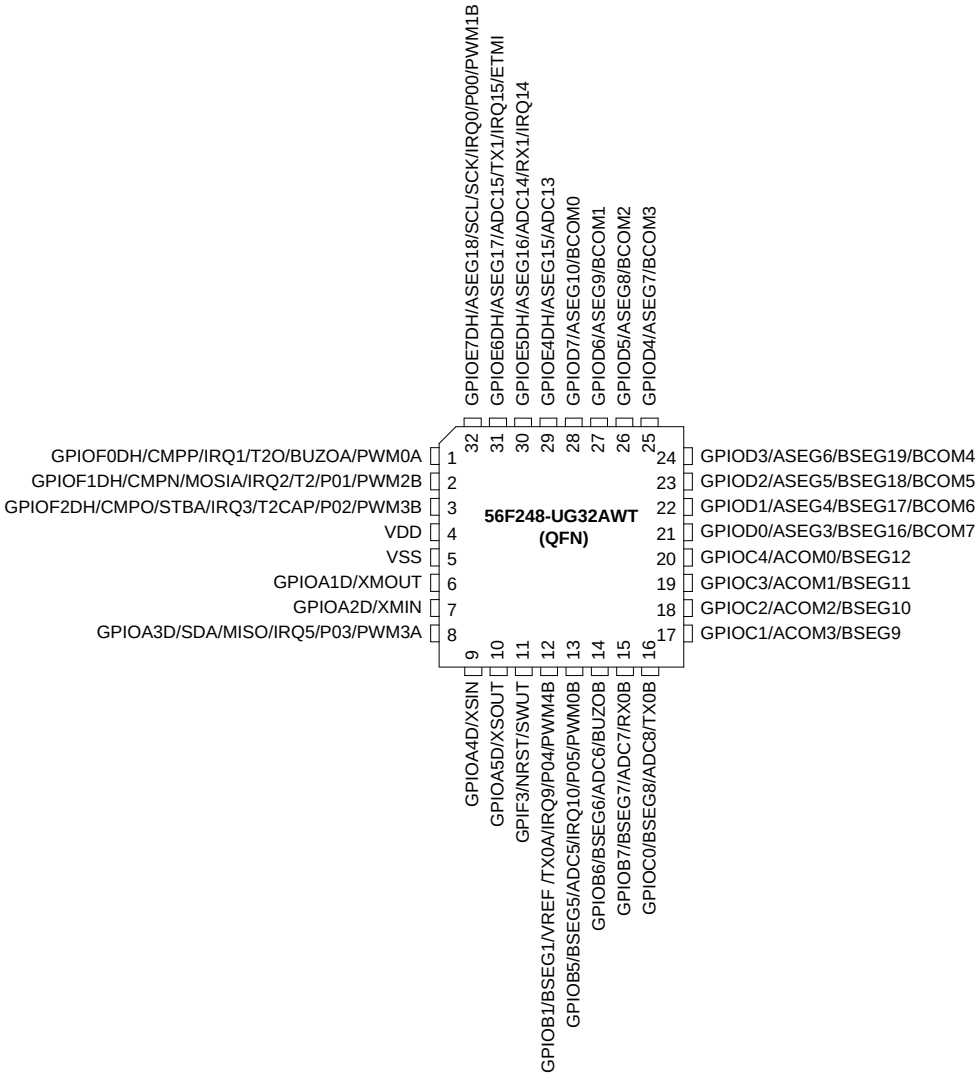
4. Pin Configuration

WT56F248-RG64A WT 64-Pin LQFP (WT56F232 is the same)



WT56F248-RG44A WT 44-Pin LQFP (WT56F232 is the same)

WT56F248-UG32AWT 32-Pin QFN (WT56F232 is the same)



4.1 Pin Description

4.1.1 44-Pin LQFP pin descriptions

Pin Number			Pin Name		Primary Functions	
RG64A WT	RG44A WT	UG32A WT		I/O	Descriptions	Circuit Type
1	2	1	GPIOF0DH/ CMPP/ IRQ1/ T2O/ BUZOA/ PWM0A	I/O	GPIOF0DH: General-purpose I/O with programmable high current sink/source push-pull or open drain CMPP: Comparator Positive Input pin IRQ1: External Interrupt Request 1 T2O: Timer 2 Overflow Output pin BUZOA: Buzzer Output pin of Path A PWM0A: PWM0A Output pin of Path A	C1
2	3	2	GPIOF1DH/ CMPN/ MOSIA/ IRQ2/ T2/ P01/ PWM2B	I/O	GPIOF1DH: General-purpose I/O with programmable high current sink/source push-pull or open drain CMPN: Comparator Negative Input pin MOSIA: MOSI pin of Path A of SPI IRQ2: External Interrupt Request 2 T2: Timer 2 External Input pin P01: Mapping to 8052 P0.1 PWM2B: PWM2B Output pin of Path B	C1
3	4	3	GPIOF2DH/ CMPO/ STBA/ IRQ3/ T2CAP/ P02/ PWM3B	I/O	GPIOF2DH: General-purpose I/O with programmable high current sink/source push-pull or open drain CMPO: Comparator Output pin STBA: STB pin of Path A of SPI IRQ3: External Interrupt Request 3 T2CAP: Timer 2 Capture Input pin P02: Mapping to 8052 P0.2 PWM3B: PWM3 Output pin of Path B	A
4			GPIOG3/ IRQ2B/ P06/ PWM4A		GPIOG3: General-purpose I/O with push-pull IRQ2B: External Interrupt Request 2 of Path B P06: Mapping to 8052 P0.6 PWM4A: PWM4 output pin of Path A	A
5			GPIOG4/ IRQ3B/ P07/ PWM5A		GPIOG4: General-purpose I/O with push-pull IRQ3B: External Interrupt Request 3 of Path B P07: Mapping to 8052 P0.7 PWM5A: PWM5 output pin of Path A	A
6			GPIOG5		GPIOG5: General-purpose I/O with push-pull	A2
7	5	4	VDD	PWR	VDD power	
8	6	5	VSS	GND	Core ground	
9			GPIOA0D/ MOSIB/ IRQ4	I/O	GPIOA0D: General-purpose I/O with programmable push-pull or open drain MOSIB: MOSI pin of Path B of SPI IRQ4: External Interrupt Request 4	A
10	7	6	GPIOA1D	I/O	GPIOA1D: General-purpose I/O with programmable push-pull or open drain	B3 (A3)
11	7	6	XMOUT		XMOUT: Output pin of main external oscillator	B3 (B1)

Pin Number			Pin Name		Primary Functions	
RG64A WT	RG44A WT	UG32A WT		I/O	Descriptions	Circuit Type
12	8	7	XMIN		XMIN: Input pin of main external oscillator	B3 (B1)
13	8	7	GPIOA2D	I/O	GPIOA2D: General-purpose I/O with programmable push-pull or open drain	B3 (A3)
14	9	8	GPIOA3D/ SDA/ MISO/ IRQ5/ P03/ PWM3A	I/O	GPIOA3D: General-purpose I/O with programmable push-pull or open drain SDA: SDA pin of I²C MISO: MISO pin of SPI IRQ5: External Interrupt Request 5 P03: Mapping to 8052 P0.3 PWM3A: PWM3 output pin of Path A	A
15	10	9	GPIOA4D	I/O	GPIOA4D: General-purpose I/O with programmable push-pull or open drain	B4 (A3)
16			NC			
17	10	9	XSIN		XSIN: Input pin of sub external oscillator	B4 (B2)
18	11	10	XSOUT		XSOUT: Output pin of sub external oscillator	B4 (B2)
19	11	10	GPIOA5D	I/O	GPIOA5D: General-purpose I/O with programmable push-pull or open drain	B4 (A3)
20	12	11	GPIF3/ NRST/ SWUT	I	GPIF3: Input pin NRST: Reset pin SWUT: Single-wire ISP/ICE interface	D
21			GPIOA6D/ STBB/ IRQ6/ PWM2A	I/O	GPIOA6D: General-purpose I/O with programmable push-pull or open drain STBB: STB pin of Path B of SPI IRQ6: External Interrupt Request 6 PWM2A: PWM2 output pin of Path A	A
22	13		GPIOA7D/ ADC0/ IRQ7/ ETMO/ PWM1A	I/O	GPIOA7D: General-purpose I/O with programmable push-pull or open drain ADC0: Analog/Digital Converter Input 0 IRQ7: External Interrupt Request 7 ETMO: Enhanced Timer/Counter Compare or Capture result Output PWM1A: PWM1 output pin of Path A	C2
23			GPIOF4DH	I/O	GPIOF4DH: General-purpose I/O with programmable push-pull or open drain	A3
24			GPIOF5DH	I/O	GPIOF5DH: General-purpose I/O with programmable push-pull or open drain	A3
25	14		GPIOB0/ ACOM7/ BSEG0/ ADC1/ RX0A/ IRQ8	I/O	GPIOB0: General-purpose I/O with push-pull ACOM7: LCD-A common 7 BSEG0: LCD-B segment 0 ADC1: Analog/Digital Converter Input 1 RX0A: Receive data input of Path A of UART0 IRQ8: External Interrupt Request 8	E1
26	15	12	GPIOB1/ BSEG1/ VREF/ TX0A/ IRQ9/ P04/	I/O	GPIOB1: General-purpose I/O with push-pull BSEG1: LCD B segment 1 VREF: Analog/Digital Converter Voltage Reference Input pin TX0A: Transmit data output of Path A of UART0	E2

Pin Number			Pin Name		Primary Functions	
RG64A WT	RG44A WT	UG32A WT		I/O	Descriptions	Circuit Type
			PWM4B		IRQ9: External Interrupt Request 9 P04: Mapping to 8052 P0.4 PWM4B: PWM4 output pin of Path B	
27	16		GPIOB2/ ACOM6/ BSEG2/ ADC2	I/O	GPIOB2: General-purpose I/O with push-pull ACOM6: LCD-A common 6 BSEG2: LCD-B segment 2 ADC2: Analog/Digital Converter Input 2	E1
28	17		GPIOB3/ ACOM5/ BSEG3/ ADC3	I/O	GPIOB3: General-purpose I/O with push-pull ACOM5: LCD-A common 5 BSEG3: LCD-B segment 3 ADC3: Analog/Digital Converter Input 3	E1
29	18		GPIOB4/ ACOM4/ BSEG4/ ADC4	I/O	GPIOB4: General-purpose I/O with push-pull ACOM4: LCD-A common 4 BSEG4: LCD-B segment 4 ADC4: Analog/Digital Converter Input 4	E1
30	19	13	GPIOB5/ BSEG5/ ADC5/ IRQ10/ P05/ PWM0B	I/O	GPIOB5: General-purpose I/O with push-pull BSEG5: LCD-B segment 5 ADC5: Analog/Digital Converter Input 5 IRQ10: External Interrupt Request 10 P05: Mapping to 8052 P0.5 PWM0B: PWM0 output pin of Path B	E3
31	20	14	GPIOB6/ BSEG6/ ADC6/ BUZOB	I/O	GPIOB6: General-purpose I/O with push-pull BSEG6: LCD-B segment 6 ADC6: Analog/Digital Converter Input 6 BUZOB: Buzzer output pin of Path B	E3
32	21	15	GPIOB7/ BSEG7/ ADC7/ RX0B	I/O	GPIOB7: General-purpose I/O with push-pull ADC7: Analog/Digital Converter Input 7 BSEG7: LCD-B segment 7 RX0B: Receive data input of Path B of UART0	E3
33			NC			
34	22	16	GPIOC0/ BSEG8/ ADC8/ TX0B	I/O	GPIOC0: General-purpose I/O with push-pull BSEG8: LCD-B segment 8 ADC8: Analog/Digital Converter Input 8 TX0B: Transmit data output of Path B of UART0	E3
35	23	17	GPIOC1/ ACOM3/ BSEG9	I/O	GPIOC1: General-purpose I/O with push-pull ACOM3: LCD-A common 3 BSEG9: LCD-B segment 9	E4
36	24	18	GPIOC2/ ACOM2/ BSEG10	I/O	GPIOC2: General-purpose I/O with push-pull ACOM2: LCD-A common 2 BSEG10: LCD-B segment 10	E4
37	25	19	GPIOC3/ ACOM1/ BSEG11	I/O	GPIOC3: General-purpose I/O with push-pull ACOM1: LCD-A common 1 BSEG11: LCD-B segment 11	E4
38	26	20	GPIOC4/ ACOM0/ BSEG12	I/O	GPIOC4: General-purpose I/O with push-pull ACOM0: LCD-A common 0 BSEG12: LCD-B segment 12	E4
39	27		GPIOC5/	I/O	GPIOC5: General-purpose I/O with push-pull	E4

Pin Number			Pin Name		Primary Functions	
RG64A WT	RG44A WT	UG32A WT		I/O	Descriptions	Circuit Type
			ASEG0/ BSEG13		ASEG0: LCD-A segment 0 BSEG13: LCD-B segment 13	
40			GPIOF6DH	I/O	GPIOF6DH: General-purpose I/O with programmable push-pull or open drain	A3
41			GPIOF7DH	I/O	GPIOF7DH: General-purpose I/O with programmable push-pull or open drain	A3
42			GPIOG	I/O	GPIOG0: General-purpose I/O with push-pull	A2
43	28		GPIOC6/ ASEG1/ BSEG14	I/O	GPIOC6: General-purpose I/O with push-pull ASEG1: LCD-A segment 1 BSEG14: LCD-B segment 14	E4
44	29		GPIOC7/ ASEG2/ BSEG15	I/O	GPIOC7: General-purpose I/O with push-pull ASEG2: LCD-A segment 2 BSEG15: LCD-B segment 15	E4
45	30	21	GPIOD0/ ASEG3/ BSEG16/ BCOM7	I/O	GPIOD0: General-purpose I/O with push-pull ASEG3: LCD-A segment 13 BSEG16: LCD-B segment 16 BCOM7: LCD-B common 7	E4
46	31	22	GPIOD1/ ASEG4/ BSEG17/ BCOM6	I/O	GPIOD1: General-purpose I/O with push-pull ASEG4: LCD-A segment 4 BSEG17: LCD-B segment 17 BCOM6: LCD-B common 6	E4
47	32	23	GPIOD2/ ASEG5/ BSEG18/ BCOM5	I/O	GPIOD2: General-purpose I/O with push-pull ASEG5: LCD-A segment 5 BSEG18: LCD-B segment 18 BCOM5: LCD-B common 5	E4
48			NC			
49			NC			
50	33	24	GPIOD3/ ASEG6/ BSEG19/ BCOM4	I/O	GPIOD3: General-purpose I/O with push-pull ASEG6: LCD-A segment 6 BSEG19: LCD-B segment 19 BCOM4: LCD-B common 4	E4
51	34	25	GPIOD4/ ASEG7/ BCOM3	I/O	GPIOD4: General-purpose I/O with push-pull ASEG7: LCD-A segment 7 BCOM3: LCD-B common 3	E4
52	35	26	GPIOD5/ ASEG8/ BCOM2	I/O	GPIOD5: General-purpose I/O with push-pull ASEG8: LCD-A segment 8 BCOM2: LCD-B common 2	E4
53	36	27	GPIOD6/ ASEG9/ BCOM1	I/O	GPIOD6: General-purpose I/O with push-pull ASEG9: LCD-A segment 9 BCOM1: LCD-B common 1	E4
54	37	28	GPIOD7/ ASEG10/ BCOM0	I/O	GPIOD7: General-purpose I/O with push-pull ASEG10: LCD-A segment 10 BCOM0: LCD-B common 0	E4
55			GPIOG1/ IRQ0B	I/O	GPIOG1: General-purpose I/O with push-pull IRQ0B: External Interrupt Request 0 of Path B	A4
56			GPIOG2/ IRQ1B	I/O	GPIOG2: General-purpose I/O with push-pull IRQ1B: External Interrupt Request 1 of Path B	A4

Pin Number			Pin Name		Primary Functions	
RG64A WT	RG44A WT	UG32A WT		I/O	Descriptions	Circuit Type
57	38		GPIOE0DH/ ASEG11/ ADC9	I/O	GPIOE0DH: General-purpose I/O with programmable high current sink/source push-pull or open drain ASEG11: LCD-A segment 11 ADC9: Analog/Digital Converter Input 9	E6
58	39		GPIOE1DH/ ASEG12/ ADC10/ IRQ11	I/O	GPIOE1DH: General-purpose I/O with programmable high current sink/source push-pull or open drain ASEG12: LCD-A segment 12 ADC10: Analog/Digital Converter Input 10 IRQ11: External Interrupt Request 11	E6
59	40		GPIOE2DH/ ASEG13/ ADC11/ IRQ12/ PWM5B	I/O	GPIOE2DH: General-purpose I/O with programmable high current sink/source push-pull or open drain ASEG13: LCD-A segment 13 ADC11: Analog/Digital Converter Input 11 IRQ12: External Interrupt Request 12 PWM5B: PWM5 output pin of Path B	E6
60	41		GPIOE3DH/ ASEG14/ ADC12/ IRQ13/ BUZOC	I/O	GPIOE3DH: General-purpose I/O with programmable high current sink/source push-pull or open drain ASEG14: LCD-A segment 14 ADC12: Analog/Digital Converter Input 12 IRQ13: External Interrupt Request 13 BUZOC: Buzzer output pin of Path C	E6
61	42	29	GPIOE4DH/ ASEG15/ ADC13	I/O	GPIOE4DH: General-purpose I/O with programmable high current sink/source push-pull or open drain ASEG15: LCD-A segment 15 ADC13: Analog/Digital Converter Input 13	E6
62	43	30	GPIOE5DH/ ASEG16/ ADC14/ RX1/ IRQ14	I/O	GPIOE5DH: General-purpose I/O with programmable high current sink/source push-pull or open drain ASEG16: LCD-A segment 16 ADC14: Analog/Digital Converter Input 14 RX1: Receive data input of UART1 IRQ14: External Interrupt Request 14	E6
63	44	31	GPIOE6DH/ ASEG17/ ADC15/ TX1/ IRQ15/ ETMI	I/O	GPIOE6DH: General-purpose I/O with programmable high current sink/source push-pull or open drain ASEG17: LCD-A segment 17 ADC15: Analog/Digital Converter Input 15 TX1: Transmit data output of UART1 IRQ15: External Interrupt Request 15 ETMI: Enhanced Timer/Counter Clock Source or Capture Input	E6
64	1	32	GPIOE7DH/ ASEG18/ SCL/ SCK/	I/O	GPIOE7DH: General-purpose I/O with programmable high current sink/source push-pull or open drain ASEG18: LCD-A segment 18	A1

Pin Number			Pin Name		Primary Functions	
RG64A WT	RG44A WT	UG32A WT		I/O	Descriptions	Circuit Type
			IRQ0/ P00/ PWM1B		SCL: SCL pin of I²C SCK: SCK pin of SPI IRQ0: External Interrupt Request 0 P00: Mapping to 8052 P0.0 PWM1B: PWM1 output pin of Path B	

Note 1: All I/O pins are floating on Reset status.

Note 2: While using 8052 port (P0.x), please set the mapping rGPIO_TYP as open drain and connect to external pull-up resistor.

Note 3: While using UART0, please connect to the external pull-up resistor.

Note 4: While using UART1 or I^2C, please set the mapping rGPIO_TYP as open drain and connect to external pull-up resistor.

4.2 Pin Summary

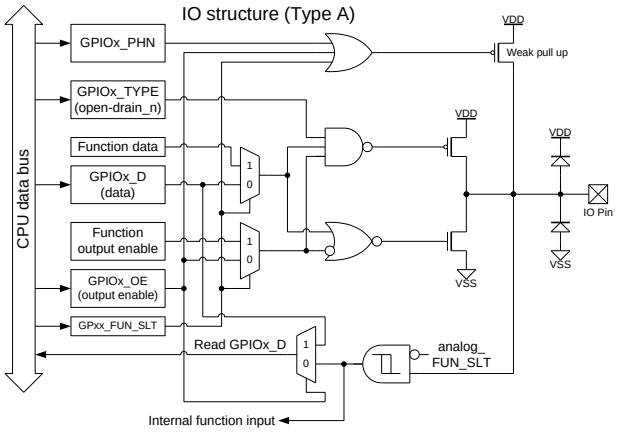
Explain each pin function in details.

Pin Name	Type	Description
PORT		
GPIOA0 ~ GPIOA7	I/O	8-bit bidirectional general-purpose I/O port
GPIOB0 ~ GPIOB7	I/O	8-bit bidirectional general-purpose I/O port
GPIOC0 ~ GPIOC7	I/O	8-bit bidirectional general-purpose I/O port
GPIOD0 ~ GPIOD7	I/O	8-bit bidirectional general-purpose I/O port
GPIOE0 ~ GPIOE7	I/O	8-bit bidirectional general-purpose I/O port
GPIOF0 ~ GPIF7	I/O	8-bit bidirectional general-purpose I/O port (GPIF3 is input only pin)
GPIOG0 ~ GPIG5	I/O	6-bit bidirectional general-purpose I/O port
Timer2		
T2O	O	Timer/Counter 2 Overflow Output
T2	I	Timer/Counter 2 External Input
T2CAP	I	Timer/Counter 2 Capture Input (each Falling Edge)
Enhanced Timer/Counter		
ETMO	O	Enhanced Timer/Counter Compare Result Output
ETMI	I	Enhanced Timer/Counter Clock Source or Capture Input
Buzzer		
BUZOA	O	Buzzer Output of Path A
BUZOB	O	Buzzer Output of Path B
BUZOC	O	Buzzer Output of Path C
IRQ		
IRQ0 ~ IRQ15	I	16 External Interrupt Request Input pins
PWM		
PWM0 A/B	O	PWM 0 Output of Path A or Path B
PWM1 A/B	O	PWM 1 Output of Path A or Path B
PWM2 A/B	O	PWM 2 Output of Path A or Path B
PWM3 A/B	O	PWM 3 Output of Path A or Path B
PWM4 A/B	O	PWM 4 Output of Path A or Path B
PWM5 A/B	O	PWM 5 Output of Path A or Path B
UART		
RX0 A/B	I	UART0 Receive Path A or Path B
TX0 A/B	O	UART0 Transmit Path A or Path B
RX1	I	UART1 Receive
TX1	O	UART1 Transmit
SPI		
SCK	I/O	SPI interface clock
MOSIA	I/O	SPI data pin MOSI (Master Output; Slave Input) of Path A
STBA	O	SPI Enable of Path A
MISO	I/O	SPI Data pin MISO (Master Input; Slave Output)

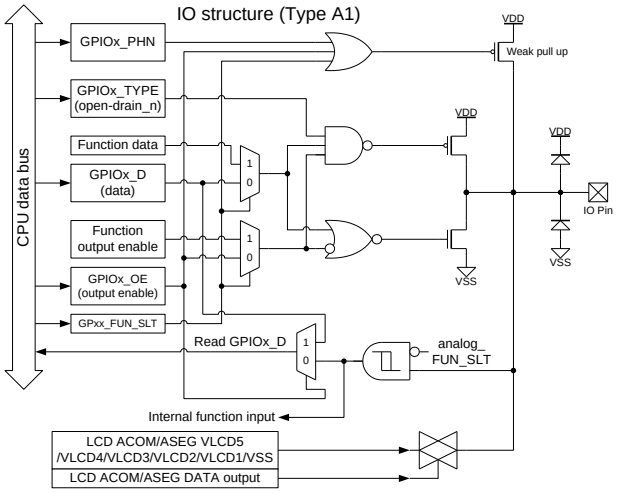
Pin Name	Type	Description
MOSIB	I/O	SPI Data pin MOSI (Master Output; Slave Input) of Path B
STBB	O	SPI Enable of Path B
ADC		
ADC0 ~ ADC15	I	16 Analog/Digital Input pin
ACOMP		
CMPP	I	Comparator Positive Input pin
CMPN	I	Comparator Negative Input pin
CMPO	O	Comparator Output pin
LCD		
ASEG0 ~ ASEG18	O	LCD driver A SEGMENT
ACOM0 ~ ACOM7	O	LCD driver A COM
BSEG0 ~ BSEG19	O	LCD driver B SEGMENT
BCOM0 ~ BCOM7	O	LCD driver B COM
I²C		
SCL	I/O	I²C interface clock
SDA	I/O	I²C interface data
VCC & VSS		
VDD	P	Power
VSS	P	Ground
OSC		
XMOUT	O	Main crystal oscillator output
XMIN	I	Main crystal oscillator input
XSIN	I	Sub crystal oscillator input
XSOUT	O	Sub crystal oscillator output
RESET		
NRST	I	CPU reset
ISP & ICE		
SWUT	I/O	Single-wire ISP & ICE interface

4.3 Port Structure

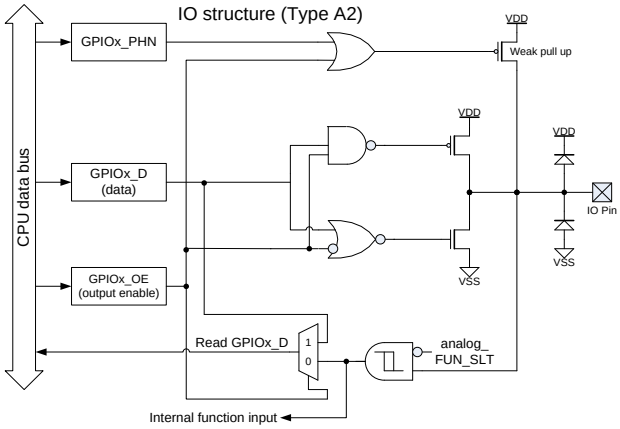
I/O Structure (Type A)



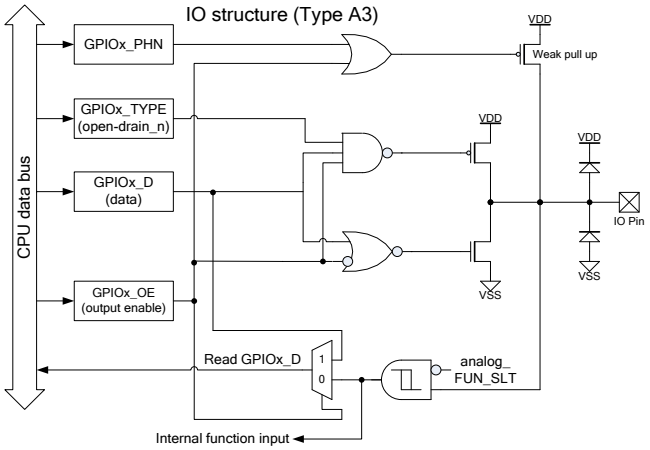
I/O Structure (Type A1)



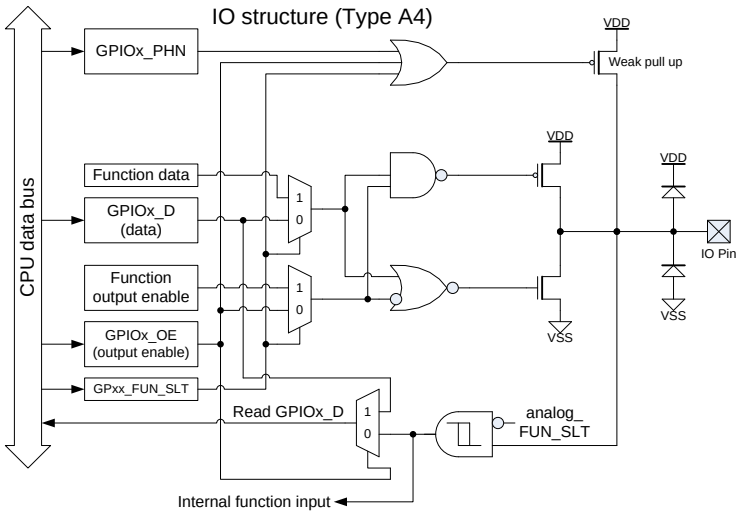
I/O Structure (Type A2)



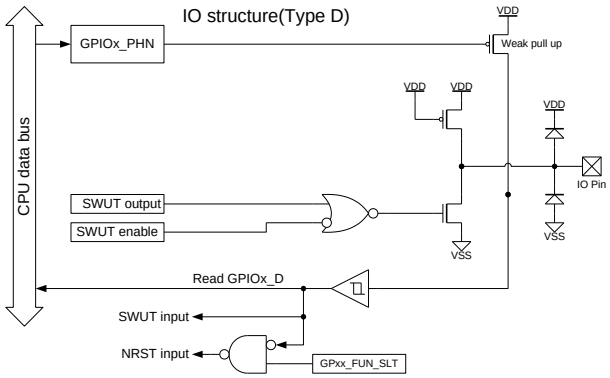
I/O Structure (Type A3)



I/O Structure (Type A4)

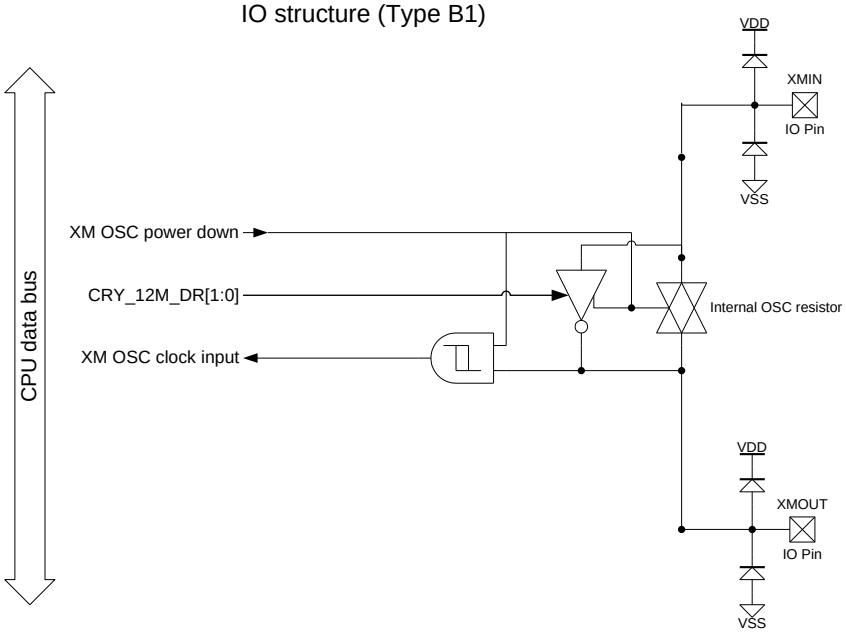


I/O Structure (Type D)



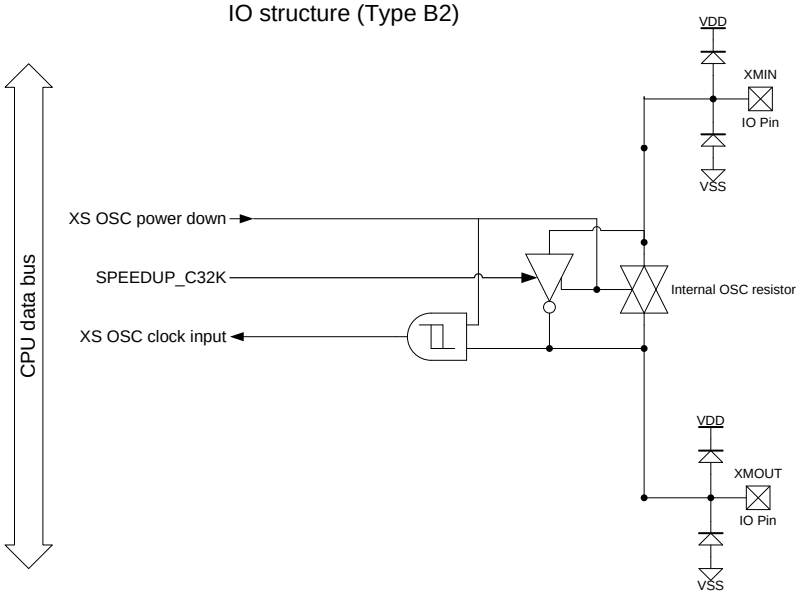
I/O Structure (Type B1)

IO structure (Type B1)

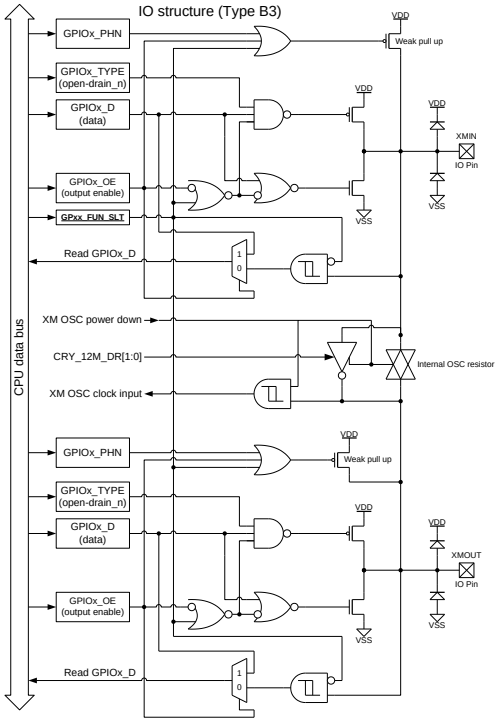


I/O Structure (Type B2)

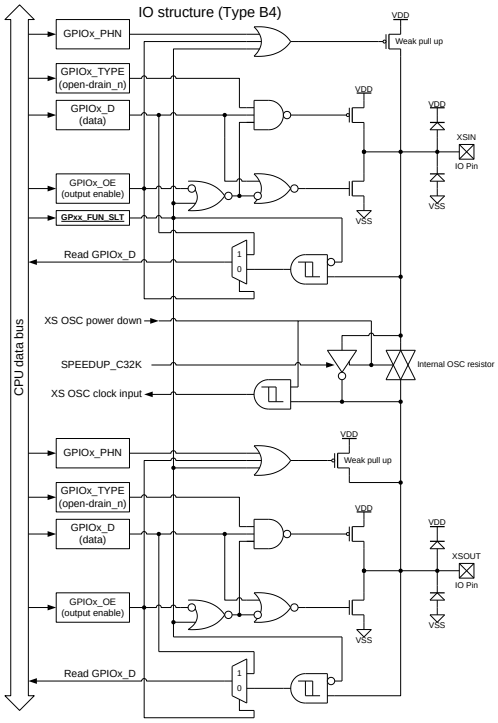
IO structure (Type B2)



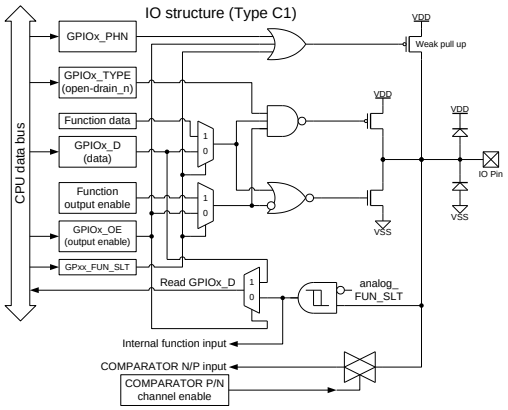
I/O Structure (Type B3)



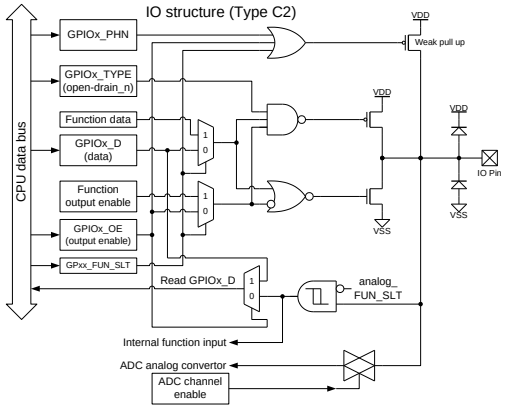
I/O Structure (Type B4)



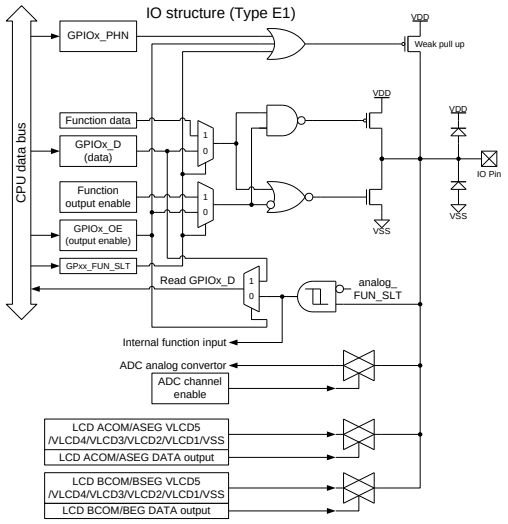
I/O Structure (Type C1)



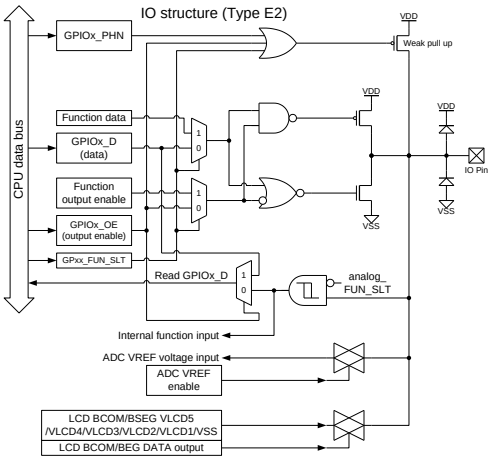
I/O Structure (Type C2)



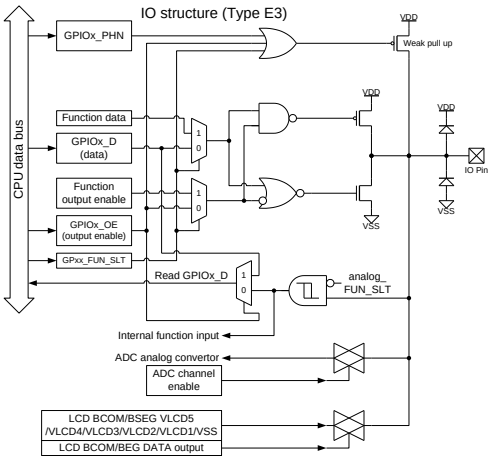
I/O Structure (Type E1)



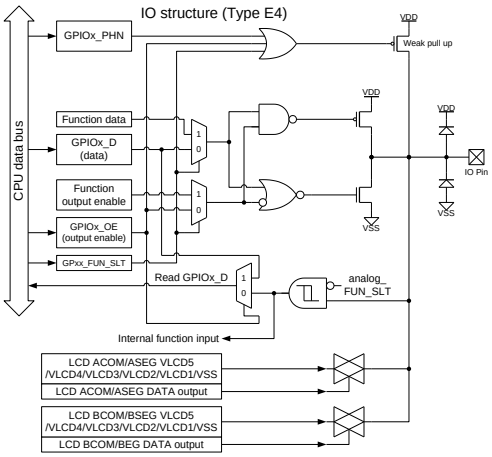
I/O Structure (Type E2)



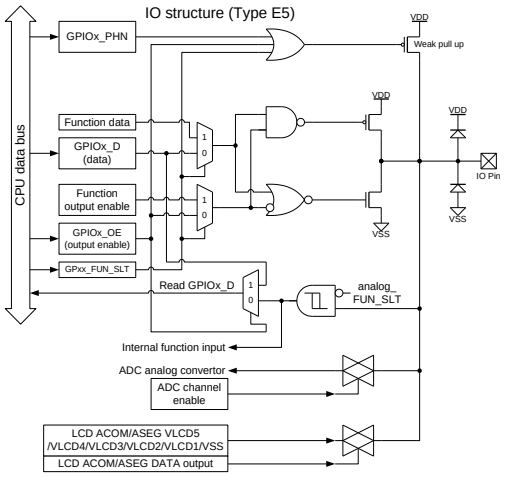
I/O Structure (Type E3)



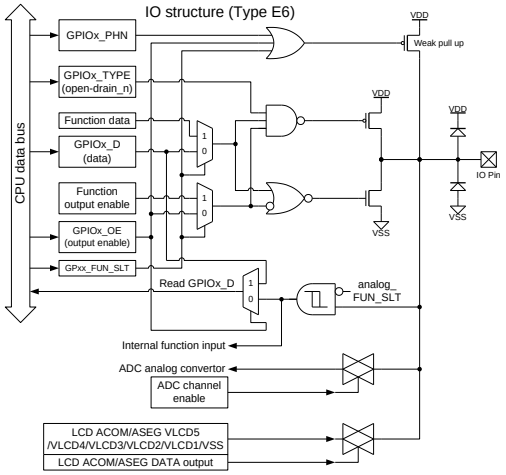
I/O Structure (Type E4)



I/O Structure (Type E5)



I/O Structure (Type E6)



5. Normal Function

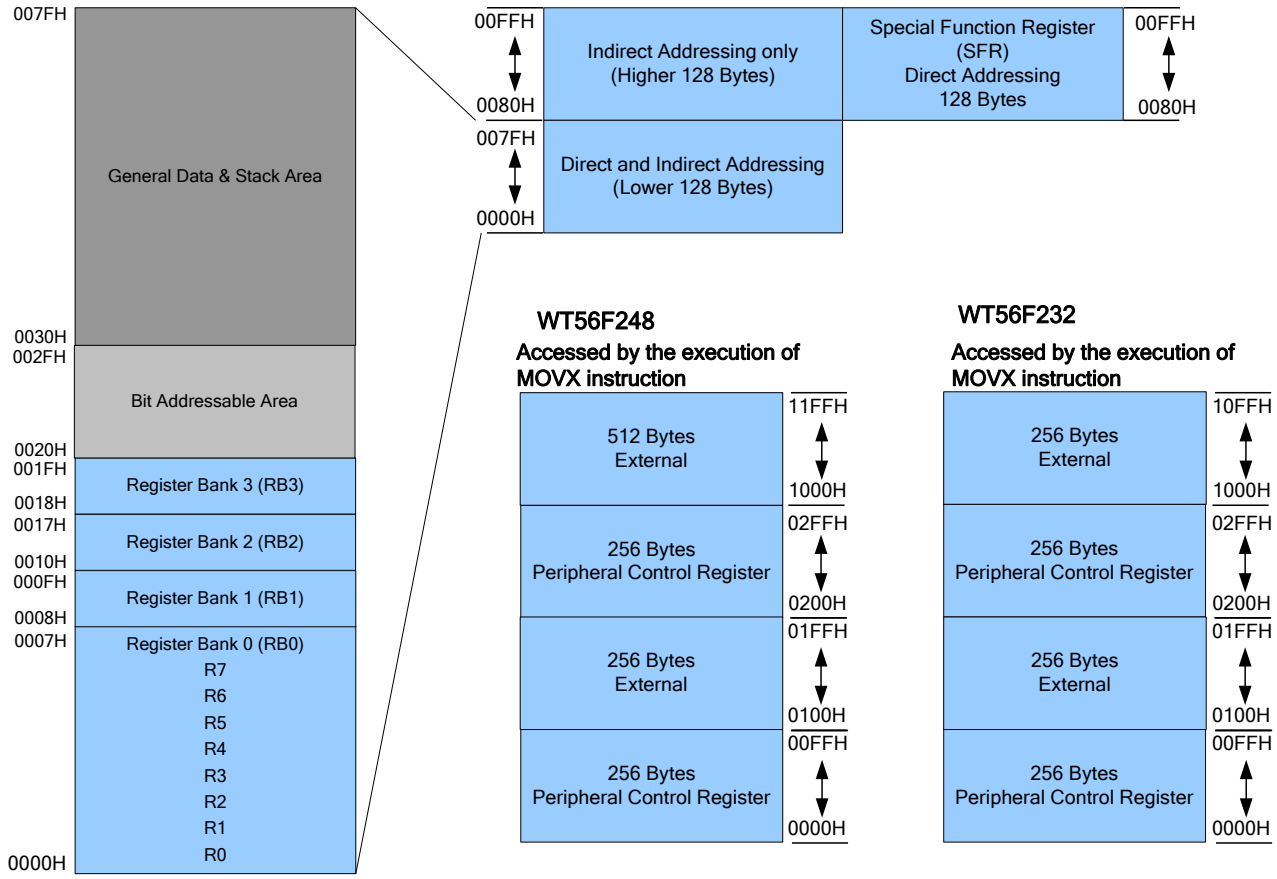
5.1 CPU

The WT56F248/232 has an embedded 8-bit 1T 8052 compatible CPU with 16-bit space addressable and 8-bit data access functions. The instruction execution time of 1T 8052 is three times faster than that of the conventional 3T 8052, and 12 times faster than that of 12T 8052. All of the functions and Special Function Register (SFR) definitions will be described in below sections.

5.2 RAM

The WT56F248/232 consists of 256+768/256+512 Bytes of SRAM. The 256 Bytes of RAM is the internal RAM of the general 8052. External 768/512 Bytes of SRAM can be accessed by the execution of MOVX instruction.

Below figure shows a map of the RAM. For Peripheral Control Registers, see section 6.1.



The internal SRAM contains:
128 Bytes of internal SRAM, locates from 0x0000H to 0x007FH (direct and indirect addressing is allowed)
128 Bytes of internal SRAM, locates from 0x0080H to 0x00FFH (indirect addressing)
WT56F248: 256+512 Bytes of external SRAM, locates from 0x0100H to 0x01FFH & 0x1000H to 0x11FFH (accessed by MOVX instruction)

WT56F232: 256+256 Bytes of external SRAM, locates from 0x0100H to 0x01FFH & 0x1000H to 0x10FFH (accessed by MOVX instruction)

Its main purpose is for storing data in the program, and therefore it is also called Data Memory. The Data memory of WT56F248/232 includes the following sections:

(1) The lower 128 bytes of internal SRAM (0000H ~ 007FH) which can be accessed by direct or indirect addressing are divided into 3 segments:

- **General Purpose Register**: Locates from 0000H to 001FH, 32 Bytes in total, can be divided into 4 register banks. Each register bank contains 8 general purpose registers (R0~R7). 4 register banks can be selected by the select bit RS1 and RS0 in the Program Status Word Register.
- **Bit Addressable Area**: Locates from 20H to 2FH, 16 Bytes in total. Each one of the 128 bits of this segment can be directly addressed by Bit Addressing.
- **General Data Area:** Locates from 0030H to 007FH, 80 Bytes are available to the user as data RAM (including the Stack area).

(2) The higher 128 bytes of internal SRAM (0080H ~ 00FFH) can be accessed by indirect addressing through R0 or R1 (*).

(3) Special Function Registers (SFR), locates from 0080H to 00FFH, can be accessed by direct addressing (*).

(4) 768/512 Bytes of external SRAM, locates from 0x0100H to 0x01FFH & 0x1000H to 0x11FFH/0x1000H to 0x10FFH, can be accessed by instruction MOVX.

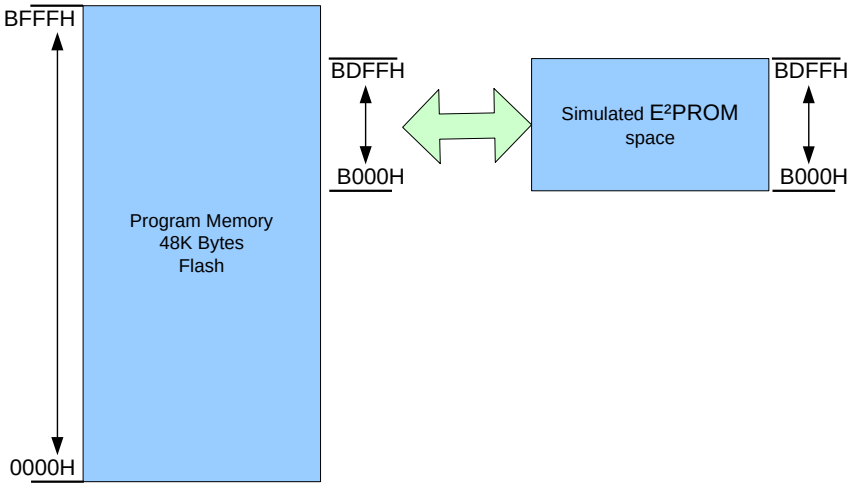
(*) Although the SFR and the higher 128 Bytes of internal RAM occupy the same addresses (0080H ~ 00FFH), they are two separate areas. MCU will automatically determine which area is in use by two different accessing ways.

5.3 Flash Memory

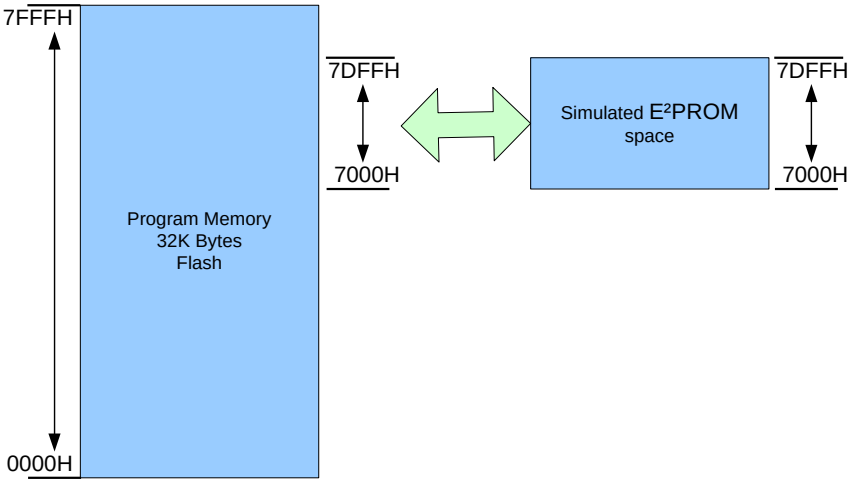
The WT56F248/232 consists of 48K/32K built-in flash, which can be served as general Program memory or simulated E^2PROM with features as below:

- ♦ FLASH memory: 48K/32K Bytes
- ♦ Operating voltage: 2.2V ~ 5.5V
- ♦ In-System Programming (ISP)
- ♦ Over 10 years Data Retention
- ♦ Read Out Protection and Code Encryption
- ♦ Emulated E^2PROM function

WT56F248 Flash Memory



WT56F232 Flash Memory



Note 1: The last 8 bytes of WT56F248 FLASH is Code Option, and the available flash ranges from 0x0000H ~ 0xBFF7H.
Note 2: The last 8 bytes of WT56F232 FLASH is Code Option, and the available flash ranges from 0x0000H ~ 0x7FF7H.

5.4 Memory Mapping

WT56F248/232 built-in 128 Bytes of direct addressing 8052 standard Special Function Register (SFR), as described below.

- CPU Core Register: ACC, B, PSW, SP, DPL0, DPH0, DPL1, DPH1, DPS
- Interrupt Register: IP, IE, XICON
- I/O port Register: P0
- Timer Register: TCON, TMOD, TL0, TH0, TL1, TH1, T2CON, T2MOD, TL2, TH2, RCAP2L, RCAP2H
- UART0 Register: SCON0, SBUF0, SBRG0H, SBRG0L, PCON
- UART1 Register: SCON1, SBUF1, SBRG1H, SBRG1L

Special Function Register (SFR) MAP:

	Bit Addressable	No Bit Addressable							
F8H									FFH
F0H	B								F7H
E8H									EFH
E0H	ACC								E7H
D8H	SCON1	SBUF1	SBRG1H	SBRG1L					DFH
D0H	PSW								D7H
C8H	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2			CFH
C0H	XICON								C7H
B8H	IP								BFH
B0H									B7H
A8H	IE								AFH
A0H									A7H
98H	SCON0	SBUF0	SBRG0H	SBRG0L					9FH
90H									97H
88H	TCON	TMOD	TL0	TL1	TH0	TH1			8FH
80H	*P0*	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON	87H

Special Function Register (SFR) Table:

Register Name	Address	Reset Value	Description
P0	80H	FFh	Port 0
SP	81H	07h	Stack Pointer
DPL0	82H	00h	Data Pointer 0 low byte
DPH0	83H	00h	Data Pointer 0 high byte
DPL1	84H	00h	Data Pointer 1 low byte
DPH1	85H	00h	Data Pointer 1 high byte
DPS	86H	00h	Data Pointer select
PCON	87H	00h	Power Control Register
TCON	88H	00h	Timer 0/1 Counter Control
TMOD	89H	00h	Timer 0/1 Mode Control

Register Name	Address	Reset Value	Description
TL0	8AH	00h	Timer 0, low byte
TL1	8BH	00h	Timer 1, low byte
TH0	8CH	00h	Timer 0, high byte
TH1	8DH	00h	Timer 1, high byte
SCON0	98H	00h	Serial Port 0, Control Register
SBUF0	99H	00h	Serial Port 0, Data Buffer
SBRG0H	9AH	00h	Serial Baud rate Generator, high byte
SBRG0L	9BH	00h	Serial Baud rate Generator, low byte
IE	A8H	00h	Interrupt Enable Register
IP	B8H	00h	Interrupt Priority Register 1
XICON	C0H	00h	Interrupt Enable Register (INT2/INT3)
T2CON	C8H	00h	Timer 2 Control
T2MOD	C9H	00h	Timer 2 Mode Control
RCAP2L	CAH	00h	Compare/Reload/Capture Register, low byte
RCAP2H	CBH	00h	Compare/Reload/Capture Register, high byte
TL2	CCH	00h	Timer 2, low byte
TH2	CDH	00h	Timer 2, high byte
PSW	D0H	00h	Program Status Word
SCON1	D8H	00h	Serial Port 1, Control Register
SBUF1	D9H	00h	Serial Port 1, Data Buffer
SBRG1H	DAH	00h	Serial Baud rate Generator 1, high byte
SBRG1L	DBH	00h	Serial Baud rate Generator 1, low byte
ACC	E0H	00h	Accumulator
B	F0H	00h	B Register

Note: Refer to 5.7 "Reset" section for the initial value of SFR.

Introduction of WT56F248/232 CPU SFR is as below:

B: Address: F0H **Reset Value: 00h**

7	6	5	4	3	2	1	0
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

The B register is used during multiply and divide operations. It can store the multiplier and the high bytes of operation result in multiply operation, and also the divisor and the remainder of operation result in divide operation. The B register can be used as a general register.

ACC: Address: E0H **Reset Value: 00h**

7	6	5	4	3	2	1	0
ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

ACC is the Accumulator register, used for data operations.

P0: Address: 80H **Reset Value: FFh**

7	6	5	4	3	2	1	0
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Data setting of Output/Input port P0.

PSW (Program Status Word): Address: D0H **Reset Value: 00h**

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	F1	PARITY

The Program Status Word contains program status information.

Bit Number	Bit Mnemonic	Description
7	CY	Carry Flag, used to indicate the result of arithmetic operation whether a carry or borrow occurred in the 7th bit. Operation result of Addition: CY = 1: a carry occurred; CY = 0: no carry occurred. Operation result of Subtraction: CY = 1: a borrow occurred; CY = 0: no borrow occurred.
6	AC	Auxiliary-Carry Flag, used to indicate the result of arithmetic operation whether the 3rd bit borrow (or carry) from the 4th bit occurred. Operation result of Addition: AC = 1: a carry occurred; AC = 0: no carry occurred. Operation result of Subtraction: AC = 1: a carry occurred; AC = 0: no carry occurred.
5	F0	General purpose flag, can be served as common read/write bit.
4	RS1	Register Bank Select bits 1 and 0 (refer to Register Bank Selection Table).
3	RS0	
2	OV	Overflow Flag, used to indicate the result of arithmetic operation whether an overflow occurred. If OV = 1, an overflow occurred. Otherwise, it is cleared.
1	F1	General-purpose flag, can be served as common read/write bit.
0	P	Parity Flag. It is set to indicate an odd number of “1” bits in the accumulator. Otherwise, it is cleared.

Register Bank Selection Table:

Register Bank	Address	RS1	RS0
0	00H-07H	0	0
1	08H-0FH	0	1
2	10H-17H	1	0
3	18H-1FH	1	1

SP (Stack Point) Address: 81H **Reset Value: 07h**

7	6	5	4	3	2	1	0
SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Stack Pointer, indicated the location at which the last byte was pushed onto the stack. It is incremented before data is stored during PUSH.

DPL0 (DPTR0, low byte of the 16-bit data pointer 0) Address: 82H **Reset Value: 00h**

7	6	5	4	3	2	1	0
DPL0.7	DPL0.6	DPL0.5	DPL0.4	DPL0.3	DPL0.2	DPL0.1	DPL0.0

DPL0 is a low byte of DPTR0, using together with the data pointer of DPH0.

DPH0 (DPTR0, high byte of the 16-bit data pointer 0) Address: 83H **Reset Value: 00h**

7	6	5	4	3	2	1	0
DPH0.7	DPH0.6	DPH0.5	DPH0.4	DPH0.3	DPH0.2	DPH0.1	DPH0.0

DPH0 is a high byte of DPTR0, using together with the data pointer of DPL0.

DPL1 (DPTR1, low byte of the 16-bit data pointer 1) Address: 84H **Reset Value: 00h**

7	6	5	4	3	2	1	0
DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0

DPL1 is low byte of DPTR1, using together with the data pointer of DPH1.

DPH1 (DPTR1, high byte of the 16-bit data pointer 1) Address: 85H **Reset Value: 00h**

7	6	5	4	3	2	1	0
DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0

DPH1 is a high byte of DPTR1, using together with the data pointer of DPL1.

DPS (Data point select) Address: 86H **Reset Value: 00h**

7	6	5	4	3	2	1	0
							DPS

Data Point selection: If DPS = 0, selects DPTR0 (DPH0, DPL0)
If DPS = 1, selects DPTR1 (DPH1, DPL1)

Note: Other special function registers will be discussed in later sections.

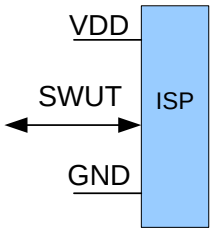
5.5 In-System Programming (ISP) (Important!!! Must Read!!!)

In-System Programming function allows users to perform programming on the target board directly without removing any components.

ISP interface adopts:

3-wire: VDD, GND (VSS), SWUT
2-wire: SWUT, GND (VSS), if the target board already has VDD power.

The figure below illustrates pins of ISP interface:



Note: See WT56F248/232 WLINK-SWUT ISP User's Manual for more details.

5.5.1 In-System Programming Notice

Condition: When MCU SOURCE clock is 12 MHz (Internal/External Oscillator), it is stable to proceed In-System Programming. For more details, please refer to Chapter 8 Application Circuits.

Description: Since this series of MCU adopts single-wire UART (SWUT) for system programming and the baud rate is 115200 bps, SOURCE clock of WT56F248/232 must work at Internal Oscillator (12 MHz) or External Oscillator (4~24 MHz).
In addition, the default setting of WT56F248/232 is IRC 12 MHz, and thus direct In-System Programming is supported. It requires adding trigger or wakeup conditions if WT56F248/232 works at Internal RC Oscillator (24 MHz), External Oscillator (< 4 MHz, 32768 Hz), Green Mode, Idle Mode or Sleep Mode, otherwise programming procedures will fail. The following section will explain how to operate in those modes. (For more details on reference clock source, please refer to section 3.1.)

GPIOxx/RESET/SWUT pin supports Reset/Input/Programming function at the same time, but each level is different. Please refer to the table below.

Function (V_{DD} = 5.0V)	VIH	VIL
SWUT	0.83 VDD	0.57 VDD
NRST	0.45 VDD	0.24 VDD

Function (V_{DD} = 3.5V)	VIH	VIL
SWUT	0.81 VDD	0.52 VDD
NRST	0.49 VDD	0.27 VDD

The programming voltage of SWUT ranging between 2.2V and 5.5V. If the programming voltage is below 2.7V, the internal pull high of GPIF3 pin must be disabled. (XFR 0x21 GPIOF_PHN[3])

Normal Mode:

If the SOURCE clock of WT56F248/232 works at Internal Oscillator (12 MHz) or External Oscillator (4~24 MHz), and WT56F248/232 performs Power On Reset normally, the programming process can go smoothly.

Please pay more attention to the following two conditions:

(1) When the SOURCE clock of WT56F248/232 selects External Oscillator and works together with particular frequency external crystal oscillator (< 4 MHz or 32.768 kHz). Since the SWUT baud rate is not 115200 bps, WT56F248/232 cannot perform programming directly.

(2) Or when the SOURCE clock of WT56F248/232 works at Internal Oscillator (24 MHz), due to the power supply with greater noises, thereby affecting the accuracy of SWUT baud rate will lead to the programming failure of WT56F248/232.

Above conditions are required to set ISP Clock Source Control Register (ISP_CHG_CTL) to enable two control bits (Bit7 ISP_CHG_12M & Bit5 UART_ISP_CHG), which allows SWUT pin to receive trigger signal. After the WT56F248/232 being switched to Internal Oscillator 12 MHz automatically, the programming process will succeed. For more details, please refer to section 6.7 (XFR_0x04 “Mandatory trigger SWUT setting procedures”).

Green Mode:

It is so-called Green Mode when MCU works at 32 kHz (Internal/External Oscillator). MCU cannot perform programming directly when works at this mode. It requires setting ISP Clock Source Control Register (ISP_CHG_CTL) to enable two control bits (Bit7 ISP_CHG_12M & Bit5 UART_ISP_CHG), which allows SWUT pin to receive trigger signal. After the MCU being switched to Internal Oscillator 12 MHz automatically, the programming process will succeed. For more details, please refer to section 6.7.

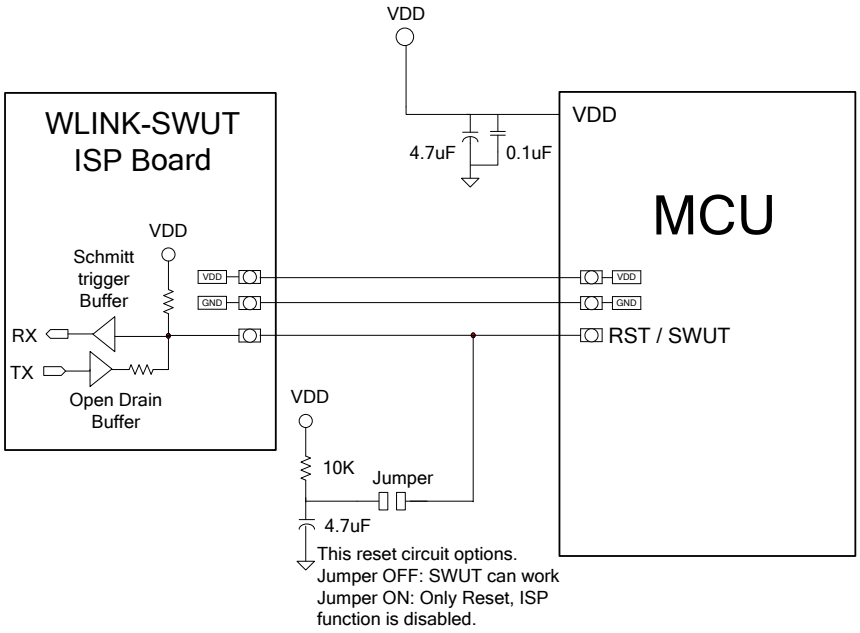
Idle Mode:

Before entering this mode, in addition to setting ISP Clock Source Control Register (ISP_CHG_CTL) to enable two control bits (Bit7 ISP_CHG_12M & Bit5 UART_ISP_CHG), be sure to set up wakeup conditions. Then MCU can switch back to work at 12 MHz, and maintain 2 ~ 3 seconds to receive the programming command from SWUT. For more details, please refer to section 6.7.

Sleep Mode:

Before entering this mode, in addition to setting ISP Clock Source Control Register (ISP_CHG_CTL) to enable two control bits (Bit7 ISP_CHG_12M & Bit5 UART_ISP_CHG), be sure to set up wakeup conditions. Then MCU can switch back to work at 12 MHz, and maintain 2 ~ 3 seconds to receive the programming command from SWUT. For more details, please refer to section 6.7.

Recommended Circuit:



5.6 Timer/Counter

The WT56F248/232 contains three 16-bit Timer/Counters (Timer0 ~ 2). All three Timer/Counters can be configured as Timer or Counter.

5.6.1 Timer/Counter0 & Timer/Counter1 (Timer 0/1)

The internal Timer/Counter 0 and Timer/Counter 1 of WT56F248/232 have four operation modes to be selected by bits M11, M10, or M01, and M00 respectively in the Special Function Register TMOD, as described below.

TMOD (8052 Timer0/1 mode control register) Address: 89H

7	6	5	4	3	2	1	0
GATE1	C1/T1	M11	M10	GATE0	C0/T0	M01	M00

Bit Number	Bit Mnemonic	Description
7	GATE1	GATE1 = 1, invalid GATE1 = 0, configured as internal Timer. If TR1 = 1, Timer1 starts.
6	C1/T1	Timer/Counter 1 selector C1/T1 = 1, invalid C1/T1 = 0, configured as an internal Timer, and the counter signal is from MCU Clock 12 MHz IRC ÷ 12
5-4	M11-M10	Timer/Counter 1 mode selection bits 00: Mode 0, 13-bit Timer/Counter 01: Mode 1, 16-bit Timer/Counter 10: Mode 2, 8-bit auto-reload Timer/Counter 11: Mode 3, Timer/Counter 1 stopped and retained count
3	GATE0	GATE0 = 1, invalid GATE0 = 0, configured as internal Timer. If TR0 = 1, Timer0 starts.

Bit Number	Bit Mnemonic	Description
2	C0/T0	Timer/Counter 0 selector C0/T0 = 1, invalid C0/T0 = 0, configured as an internal Timer, and the counter signal is from MCU Clock 12 MHz IRC ÷ 12
1-0	M01-M00	Timer/Counter 0 mode selection bits 00: Mode 0, 13-bit Timer/Counter 01: Mode 1, 16-bit Timer/Counter 10: Mode 2, 8-bit auto-reload Timer/Counter 11: Mode 3, 8-bit Timer/Counter (TL0 uses TR0 bit and TH0 uses TR1 bit)

Note: When use Timer/Counter 0 & Timer/Counter1, Cx/Tx must be set as "0" and then Timer/Counter can work normally.

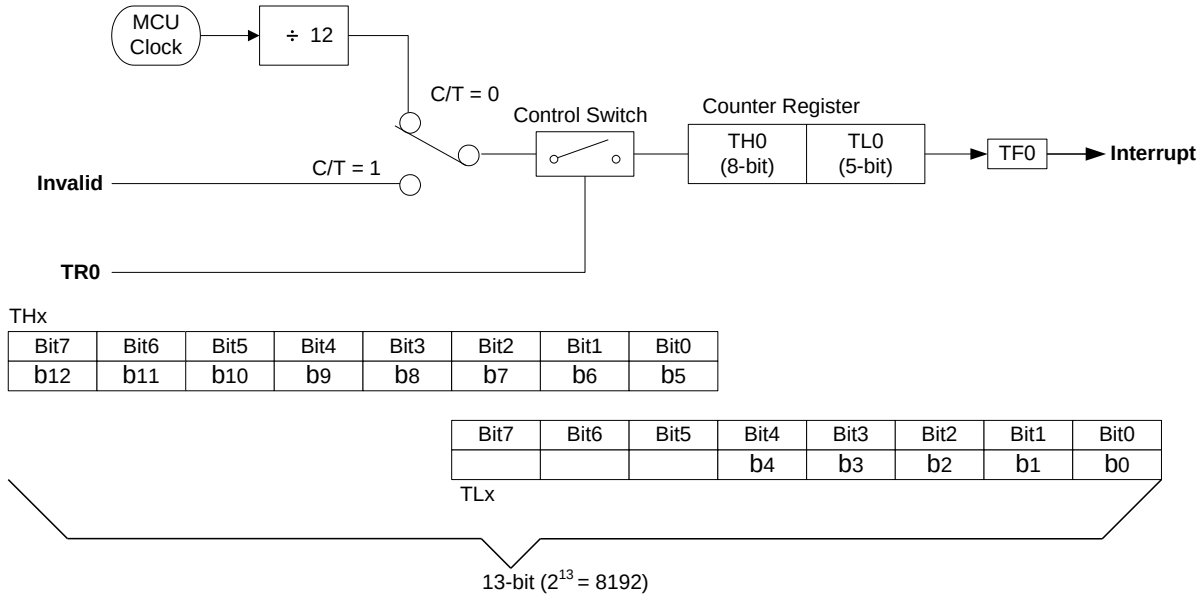
TCON (8052 Timer 0/1 control register) Address: 88H

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	-	-	-	-

Bit Number	Bit Mnemonic	Description
7	TF1	Timer/Counter 1 Overflow Flag. When the Timer/Counter overflows, TF1 is set (TF1 = 1). When CPU is jumped to the Interrupt Service Routine of Timer/Counter 1, TF1 is auto-cleared (TF1 = 0).
6	TR1	Timer/Counter 1 Enable bit. If TR1 is set (TR1 = 1), Timer/Counter 1 is in use; If TR1 is disabled (TR1 = 0), Timer/Counter 1 stopped.
5	TF0	Timer/Counter 0 Overflow Flag. When the Timer/Counter overflows, TF0 is set (TF0 = 1). When the CPU is jumped to the Interrupt Service Routine of Timer/Counter 0, TF0 is auto-cleared (TF0 = 0).
4	TR0	Timer/Counter 0 Enable bit. If TR0 is set (TR0 = 1), Timer/Counter 0 is in use; If TR0 is disabled (TR0 = 0), Timer/Counter 0 stopped.
3-0	-	Invalid

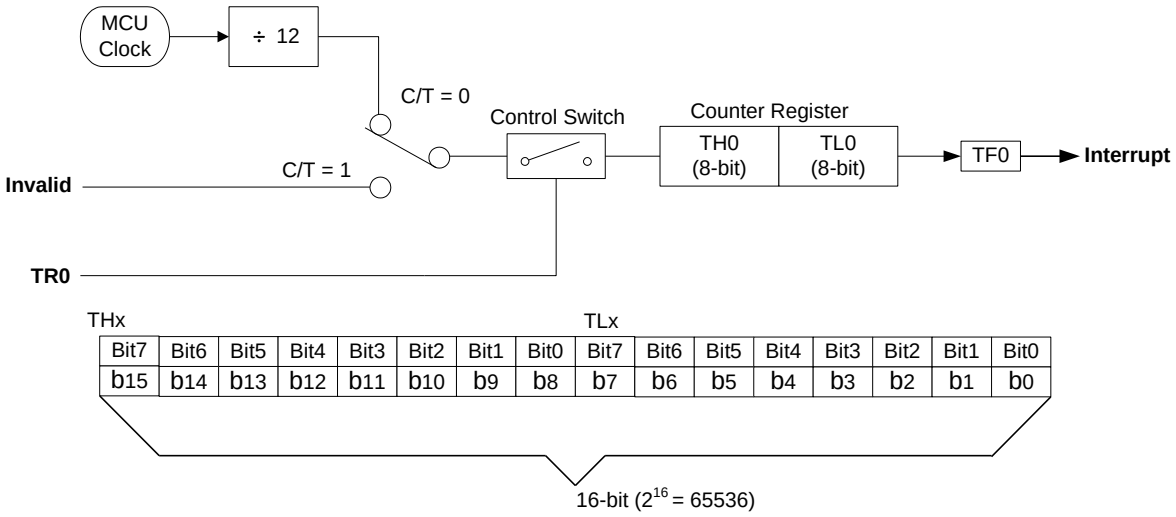
Note: See section 6.4 for more information on Baud rate generator of Timer/Counter 1.

Mode 0:



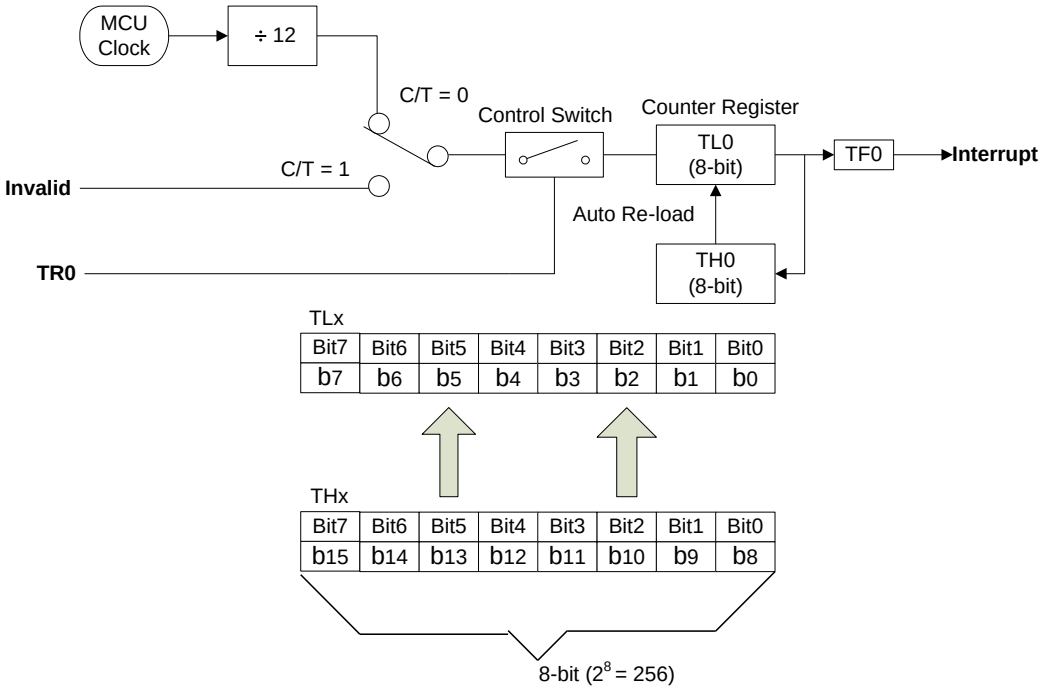
Mode 0 operation is the same for Timer/Counter 0 and Timer/Counter 1. In this mode, the timer register is configured as a 13-bit Up Timer/Counter, which is consists of the Special Function Register THx and TLx. As the count of the 13 bits is all 1s, if the register incremented 1 then count of the 13 bits is all 0s and meantime if the Timer/Counter Interrupt is enabled, an Timer overflow interrupt will occur and Overflow Flag is set (TFx = 1, and TFx locates in TCON of the Special Function Register).

Mode 1:



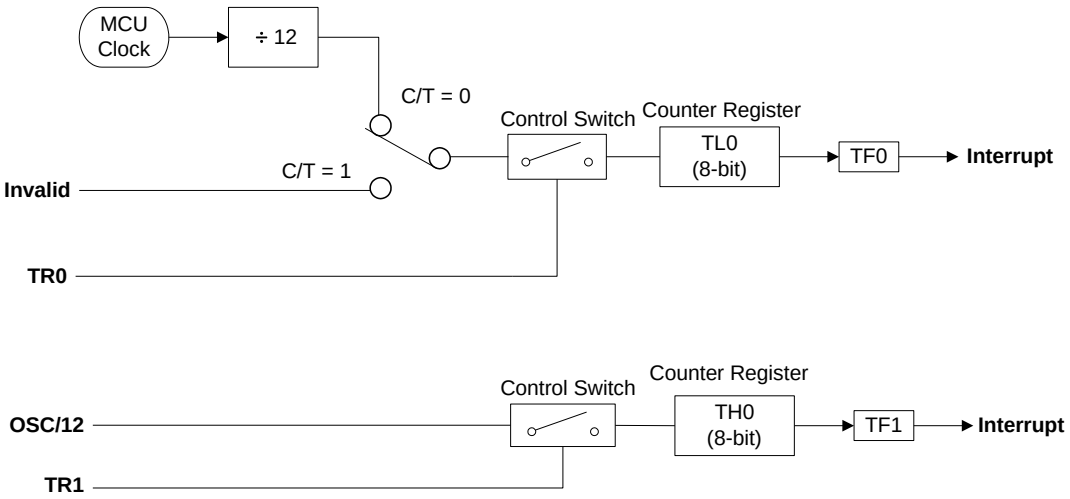
Mode 1 operation is the same as Mode 0 for Timer/Counter 0 and Timer/Counter 1, except that the Timer Register which consists of THx and TLx is configured as a 16-bit Up Timer/Counter.

Mode 2:



Mode 2 operation is the same for Timer/Counter 0 and Timer/Counter 1 to configure two 8-bit auto-reload Timer/Counters. The counter value is stored in TLx Register. Overflow from TLx not only sets TFx = 1, but also auto-reloads contents of THx to TLx.

Mode 3:



Mode 3 operation is rarely different for Timer/Counter 0 and Timer/Counter 1, as described below.
In Mode 3, TL0 is an 8-bit Timer/Counter, while TH0 is an 8-bit Counter controlled by TR1. In the meantime, be aware of the Overflow Flag of Timer/Counter 1 borrowed by TH0, and the corresponding Interrupt Service Routine address is 001BH. In Mode 3, Timer/Counter 1 stopped and retained count.

5.6.2 Timer/Counter 2 (Timer 2)

The WT56F248/232 internal Timer/Counter 2 is a 16-bit Timer/Counter. The timer/counter function can be selected by the C2/T2 bit in the Special Function Register T2CON, and the operating modes are selected by the RCLK, TCLK, CP/RL2, and TR2 bits in T2CON.

T2CON (8052 Timer 2 Control Register) Address: C8H

7	6	5	4	3	2	1	0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C2/T2	CP/RL2

Bit Number	Bit Mnemonic	Description
7	TF2	Timer 2 Overflow Flag. When Timer 2 interrupts, TF2 is set (TF2 = 1); TF2 will not be cleared until Timer 2 interrupt terminated. It must be cleared by software (setting TF2 = 0).
6	EXF2	Timer 2 External Flag bit. A capture or reload is caused by a negative transition on T2CAP (General purpose I/O port F2) if EXEN2 = 1. In addition, EXF2 bit is set (EXF2 = 1), EXF2 will not be cleared even Timer 2 interrupt terminated. It must be cleared by software (setting EXF2 = 0).
5	RCLK	UART Receive Clock bit. If RCLK = 1, selects Timer 2 overflow pulses or RCLK = 0, selects Timer 1 overflow pulses as the receive timing pulse providing for Modes 1 and 3.
4	TCLK	UART Transmit Clock bit. If TCLK = 1, selects Timer 2 overflow pulses or TCLK = 0, selects Timer 1 overflow pulses as the transmit timing pulse providing for Modes 1 and 3.
3	EXEN2	Timer 2 External Enable Control bit. When set, allows a capture or reload to occur as a result of a negative transition on T2CAP if Timer 2 is not being used to clock the UART. EXEN2 = 0 causes Timer 2 to ignore events at T2CAP.
2	TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer. TR2 = 0 stopped the timer.
1	C2/T2	Timer or Counter select bit. (Timer 2) 1 = External event counter, counts the pulse signal of T2 pin. 0 = Internal timer, counts the CPU clock pulse
0	CP/RL2	Capture/Reload Flag. CP/RL2 = 1 causes captures to occur on negative transition at T2CAP if EXEN2 = 1, and the current value in the TH2 and TL2 will be captured into RCAP2H and RCAP2L respectively. When cleared, auto reload will occur on negative transition on T2CAP if EXEN2 = 1, and the current value in the RCAP2H and RCAP2L will be reload into TH2 and TL2 respectively.

T2MOD (8052 Timer 2 Mode Control Register) Address: C9H

7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	-

Bit Number	Bit Mnemonic	Description
7-2	Reserved	-
1	T2OE	T2O output enable bit In Timer/Counter 2 Clock Out mode, connects programmable clock out to external pin (T2O).
0	Reserved	-

-: unimplemented.

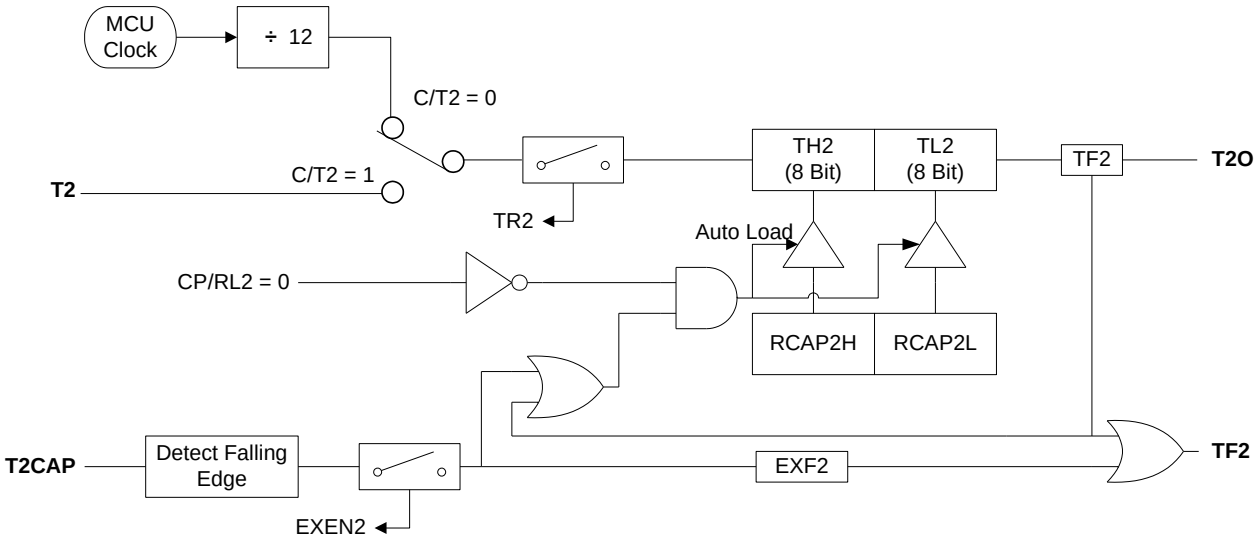
Timer/Counter 2 Operating Modes

RCLK	TCLK	CP/RL2	T2OE	Description
0	0	0	0	16-bit Auto-Reload
0	**0**	1	0	16-bit Capture
1	X	X	0	Baud Rate Generator
X	1			
X	X	0	1	Programmable Clock Out

Note: Refer to section 6.4 for more information about Timer/Counter 2 Baud Rate Generator.

Timer/Counter 2 16-bit Auto-Reload Mode

In Auto-Reload Mode, Timer 2 registers (TH2 and TL2) can be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, with the structure illustrated below.



Auto-Reload Mode is selected by the CP/RL2 bit (setting CP/RL2 = 0) in T2CON register. The Auto-Reload mode of Timer 2 is similar to Mode 2 of Timer 0/1, except that Mode 2 of Timer 0/1 is 8-bit Auto-Reload mode while Timer 2 is 16-bit Auto-Reload mode. Similarly, Auto-reload mode is allowed to count the internal clock pulse (MCU Clock/12) and also count the external input pulse from T2 pin. By setting the C/T2 bit = 0 in T2CON register, Timer 2 can operate as an internal Timer; by setting the C/T2 bit = 1 in T2CON register, Timer 2 can operate as an event counter. In addition, the EXEN2 bit in T2CON register must be set (EXEN2 = 1) to enter Auto-Reload mode. TR2 is the control bit of Timer 2. If TR2 = 1, Timer 2 is turned on; If TR2 = 0, Timer 2 is turned off.

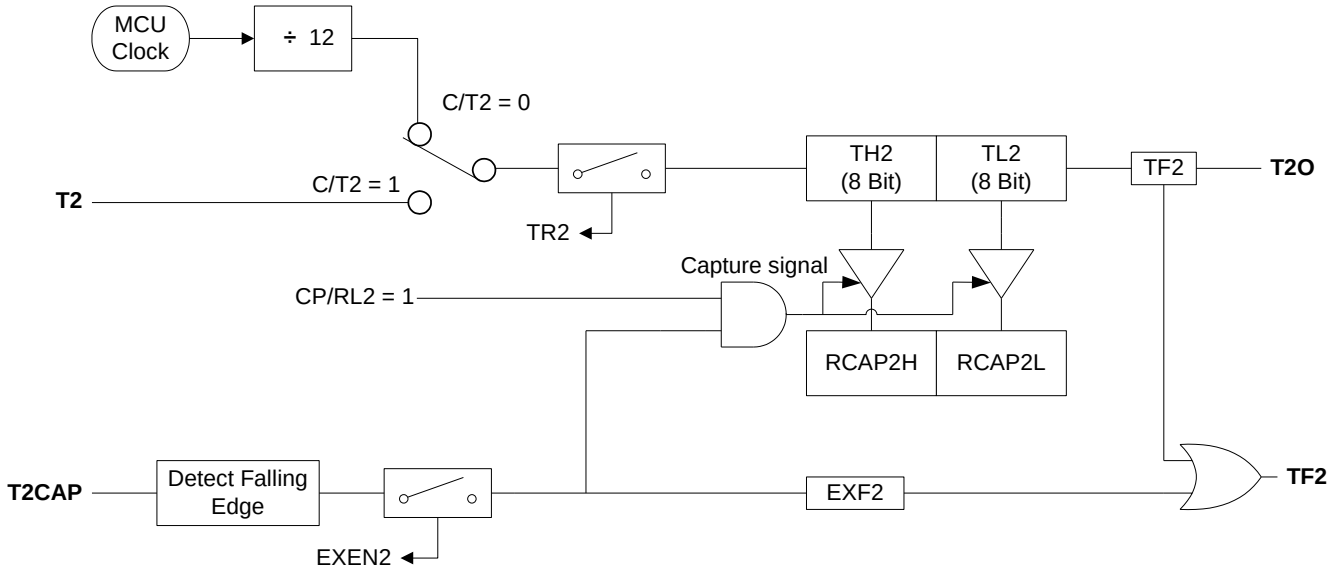
When Timer 2 is turned on, Timer 2 starts the event counting. When detected a negative transition on T2CAP, Timer 2 will auto reload the current value of RCAP2H and RCAP2L registers into TH2 and TL2 registers, respectively. In addition, EXF2 bit is set and an interrupt is generated, while the interrupt of Timer 2 will not affect the event counting. When Timer 2 counter overflows, an interrupt of Timer 2 will occur if TF2 = 1.

1. CP/RL2 = 0
2. EXEN2 = 1

If TR2 = 1, Capture mode is selected and Timer 2 starts counting. The Capture is enabled at the negative transition on T2CAP and meantime an interrupt of Timer 2 is generated. When Timer 2 counter overflows, an interrupt of Timer 2 is generated again.

Timer/Counter 2 16-bit Capture Mode

In the Capture Mode, the current value (16-bit) in timer registers TH2 and TL2 will be captured into registers RCAP2H and RCAP2L, respectively. The function block is illustrated in the figure below.



Capture Mode is selected by the CP/RL2 bit (setting CP/RL2 = 1) in T2CON register. Like Timers 0 and 1, the capture mode can count the internal clock pulse (MCU Clock/12) or the external pulse inputted from T2 pin by setting the C/T2 bit in T2CON register. If C/T2 = 0, Timer 2 can operate as an internal Timer; If C/T2 = 1, Timer 2 can operate as an external event Counter. In addition, the EXEN2 bit in T2CON register must be set (EXEN2 = 1) to enter Capture mode. TR2 is the control bit of Timer 2. If TR2 = 1, Timer 2 is turned on; If TR2 = 0, Timer 2 is turned off.

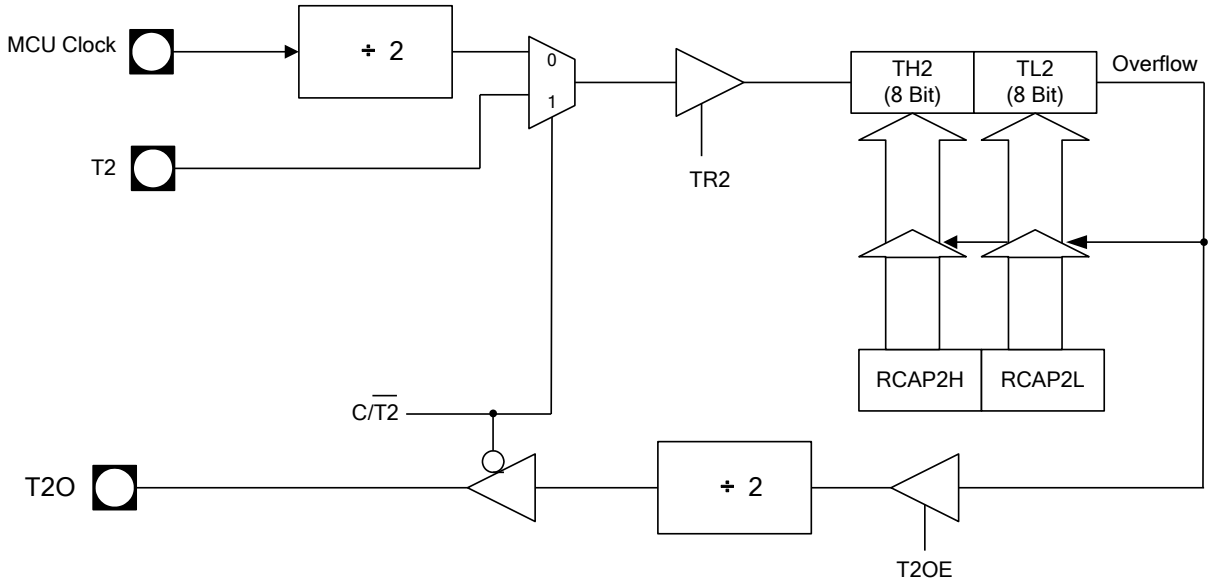
When Timer 2 is turned on, Timer 2 starts the event counting. When detected a negative transition on T2CAP, Timer 2 will capture the current value of registers TH2 and TL2 into registers RCAP2H and RCAP2L, respectively. In addition, EXF2 bit is set and an interrupt is generated, while the interrupt of Timer 2 will not affect the event counting. When Timer 2 counter overflows, an interrupt of Timer 2 will occur if TF2 = 1.

Do the following to select Capture Mode:
1. CP/RL2 = 1
2. EXEN2 = 1

If TR2 = 1, Timer 2 enters the Capture mode, and starts counting. When detected a negative transition on T2CAP input pin, the capture function is enabled and an interrupt of Timer 2 is generated. When Timer 2 counter overflows, an interrupt of Timer 2 is generated again.

Timer/Counter 2 Clock Out Mode

In the Clock Out Mode, Timer 2 registers (TH2 and TL2) can be loaded with the 16-bit value in registers RCAP2H and RCAP2L. It also functions as a 50% duty-cycle, variable-frequency clock (outputs from T2O pin), with the structure illustrated below.



Timer 2: Clock Out Mode

Clock Out Mode is selected by the CP/RL2 bit (setting CP/RL2 = 0) in T2CON register and T2OE bit (setting T2OE = 1) in T2MOD register. The output frequency is set by the 16-bit Counter which is composed of TH2 and TL2 registers.

Clock Out Mode is allowed to count the internal clock pulse (*fOSC*/2) and also count the external input pulse from T2 pin. By setting the C/T2 bit = 0 in T2CON register, Timer 2 can operate as an internal Timer; By setting the C/T2 bit = 1 in T2CON register, Timer 2 can operate as an event counter. In addition, the GPIOF0DH in GPIO Port F Complex Function Register must be set as T2O output function to enter Clock Out mode. TR2 is the control bit of Timer 2. If TR2 = 1, Timer 2 is turned on; If TR2 = 0, Timer 2 is turned off

When Timer 2 is turned on, Timer 2 starts the event counting. When detected an overflow, Timer 2 will auto reload the current value of RCAP2H and RCAP2L registers into TH2 and TL2 registers, respectively. Meanwhile, it also inverts the T2O output signal. In this mode, Timer 2 overflows will not generate interrupts.

1. CP/RL2 = 0
2. T2OE = 1
3. GPIOF0_FUN_SLT[1: 0] = 10

If TR2 = 1, Clock Out mode is selected and Timer 2 starts counting. If Timer 2 overflows, signal is auto reloaded and T2O output signal is inverted. The formula gives the Clock Out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers:

$$\text{T2O Clock Out Baud Rate} = \frac{f_{osc}}{4*(65536-[RCAP2H,RCAP2L])}$$

5.7 Reset

The WT56F248/232 has seven reset generation sources: Power On Reset (POR), Low Voltage Reset (LVR), Low Voltage Detection Reset (LVDR), External NRST pin Reset, Watchdog Reset, ISP/ICE Command Reset, and PC Counter Overflow Reset (PC_OVR). During Reset, all registers are reset to their initial values. You may judge what kind of reset is generated by Reset Flag Register (XFR 0x03).

Power-on Reset (POR)

The Power-on Reset occurs when the VDD supply voltage is below the Power-on Reset voltage threshold (refer to DC Characteristics sections for more details), then XFR: 0x03 POR_RST_FLG = 1.

Low Voltage Reset (LVR)

A reset occurs when the VDD voltage is below the operating voltage threshold, then XFR: 0x03 LVR_RST_FLG = 1.

Low Voltage Detection Reset (LVDR)

A reset occurs when the VDD voltage is below the Low Voltage Detection setting level, then XFR: 0x03 LVD_RST_FLG = 1.

External NRST pin Reset

A reset occurs when the voltage of the external reset pin (NRST) is below its VIL (refer to DC characteristics sections for more details), then XFR: 0x03 NRST_FLG = 1.

Watchdog Timer Reset

A reset occurs when the Watchdog Timer times out, then XFR: 0x03 WDT_RST_FLG = 1.

ISP/ICE Command Reset

An ISP/ICE reset occurs when SWUT pin transmitted the reset command, then XFR: 0x03 ISP_RST_FLG = 1.

PC Counter Overflow Reset (PC_OVR)

The PC counter stores the address where the current instruction locates. A reset occurs when the address exceeds the range of the Flash memory (Flash Address 0x0000 ~ 0x3FFF), then XFR: 0x03 PC_OVL_RST_FLG = 1.

Reset status

When above condition occurred, all Special Function Registers are set to their initial values. SFR contents are described in the following text. XFR contents will be discussed in next section.

The initial value of Special Function Register after Reset (as shown below):

SFR	Initial Value	SFR	Initial Value
P0	11111111b	P2	11111111b
SP	00000111b	IE	00000000b
DPL0	00000000b	P3	11111111b

SFR	Initial Value	SFR	Initial Value
DPH0	00000000b	IP	xx000000b
DPL1	00000000b	T2CON	00000000b
DPH1	00000000b	T2MOD	xxxxxx00b
DPS	00000000b	RCAP2L	00000000b
PCON	00000000b	RCAP2H	00000000b
TCON	00000000b	TL2	00000000b
TMOD	00000000b	TH2	00000000b
TL0	00000000b	PSW	00000000b
TL1	00000000b	SCON1	00000000b
TH0	00000000b	SBUF1	00000000b
TH1	00000000b	SBRG1H	00000000b
P1	11111111b	SBRG1L	00000000b
SCON0	00000000b	ACC	00000000b
SBUF0	00000000b	B	00000000b
SBRG0H	00000000b	XICON	00000000b
SBRG0L	00000000b		

5.8 System Clock and Clock sources

The WT56F248/232 contains four clock sources: DC ~ 24 MHz external crystal oscillator, external 32.768 kHz crystal oscillator, internal 12 MHz RC oscillator, and internal 32 kHz RC oscillator. The MCU clock sources are selected by External Special Function Register (XFR) SOURCE_CLK_SLT [1:0] and MCU_CLK_SLT [1:0]. The initial value is internal 12 MHz RC oscillator and without using a prescaler, at the same time MCU works at 12 MHz operating frequency. For more details, refer to section 6.7 Power Management.

Clock Sources are listed below.

Main Clock Sources	Sub Clock Sources
DC ~ 24 MHz Crystal Oscillator	32K Internal RC Oscillator
DC ~ 24 MHz Crystal Oscillator	32.768 kHz Crystal Oscillator
12M / 24 MHz Internal RC Oscillator	32K Internal RC Oscillator
12M / 24 MHz Internal RC Oscillator	32.768 kHz Crystal Oscillator

When using the Internal IRC oscillator, 12/24 MHz can be selected as MCU clock source by **HFIRC_CLK_SLT** (XFR_0x01_bit2).

IRC oscillator (12M/24M) switching procedures:
(a) IRC12M change to IRC24M
  (1) Set HFIRC_CLK_SLT
  (2) Move flash memory XDATA 0x0E07H-bit[6:0] to 0x70H register

(b) IRC24M change to IRC12M
  (1) Clear HFIRC_CLK_SLT
  (2) Move flash memory XDATA 0x0E03H-bit[6:0] to 0x70H register

6. Enhanced Function

6.1 External Special Function Register (XFR)

External Special Function Register (XFR) locates from 0x00 to 0xFF, must be accessed by the execution of MOVX instruction.

External Special Function Register table:

External memory address	Description
0000H ~ 000FH	System Register, Low Voltage Detection and Reset Register
0010H ~ 001FH	General-purpose I/O port Register
0210H ~ 0212H	
0020H ~ 002FH	General-purpose I/O port Register and Multi-function Register
0221H ~ 022DH	
0030H ~ 003FH	Interrupt Enable Register
0040H ~ 004FH	External Interrupt Request Register (IRQ)
0050H ~ 005FH	Pulse Width Modulation Register (PWM)
0250H ~ 025BH	
0060H ~ 006FH	Wakeup Register
0070H ~ 007FH	Internal Oscillator Calibration Register, Watchdog Register, Watch Timer Register
0080H ~ 008FH	LCD Driver Display Register
0090H ~ 009FH	LCD Driver Register
00A0H ~ 00AFH	I²C Serial Port Interface Register
00B0H ~ 00BFH	Enhanced Timer/Counter Register
00C0H ~ 00CFH	SPI Serial Port Interface Register
00D0H ~ 00D7H	12-bit Analog/Digital Register
00DAH ~ 00DFH	Comparator Register
00E0H ~ 00EFH	Simulated E²PROM Register

When the Reset status which is mentioned in section 5.7 occurred, the default value of external function register after reset is listed below:

Register Name	Address	Reset Default (Hex)	Index Section
Reserved	-	-	-
System Control Register	0x01	90	6.9
Low Voltage Detection Control Register	0x02	A6	6.16; 6.17
Reset Flag Register	0x03	01	6.17
ISP Clock Source Control Register	0x04	00	6.7
System Clock Source Control Register	0x05	A0	6.7
Power Saving Control Register	0x06	50	6.7
Clock Source Control Register	0x07	A3	6.7
Oscillator Driver Control Register	0x08	54	6.7
Path Selection Control Register	0x0B	00	6.7
Customer Code Register 1	0x0D	FF	6.19
Customer Code Register 2	0x0E	FF	6.19

Register Name	Address	Reset Default (Hex)	Index Section
Customer Code Register 3	0x0F	FF	6.19
General-purpose I/O Port A Output Enable Control Register	0x10	00	6.2
General-purpose I/O Port B Output Enable Control Register	0x11	00	6.2
General-purpose I/O Port C Output Enable Control Register	0x12	00	6.2
General-purpose I/O Port D Output Enable Control Register	0x13	00	6.2
General-purpose I/O Port E Output Enable Control Register	0x14	00	6.2
General-purpose I/O port F Output Enable Control Register	0x15	00	6.2
General-purpose I/O Port A Data Register	0x16	00	6.2
General-purpose I/O Port B Data Register	0x17	00	6.2
General-purpose I/O Port C Data Register	0x18	00	6.2
General-purpose I/O Port D Data Register	0x19	00	6.2
General-purpose I/O Port E Data Register	0x1A	00	6.2
General-purpose I/O Port F Data Register	0x1B	00	6.2
General-purpose I/O Port A Enable Internal Pull-up Resistor Register	0x1C	FF	6.2
General-purpose I/O Port B Enable Internal Pull-up Resistor Register	0x1D	FF	6.2
General-purpose I/O Port C Enable Internal Pull-up Resistor Register	0x1E	FF	6.2
General-purpose I/O Port D Enable Internal Pull-up Resistor Register	0x1F	FF	6.2
General-purpose I/O Port E Enable Internal Pull-up Resistor Register	0x20	FF	6.2
General-purpose I/O Port F Enable Internal Pull-up Resistor Register	0x21	FF	6.2
General-purpose I/O Port A Output Type Control Register	0x22	FF	6.2
General-purpose I/O Port E Output Type Control Register	0x23	FF	6.2
General-purpose I/O Port F Output Type Control Register	0x24	F7	6.2
General-purpose I/O Port A Complex Function Setting Register 1	0x25	00	6.2
General-purpose I/O Port A Complex Function Setting Register 2	0x26	00	6.2
General-purpose I/O Port B Complex Function Setting Register 1	0x27	00	6.2
General-purpose I/O Port B Complex Function Setting Register 2	0x28	00	6.2
General-purpose I/O Port C Complex Function Setting Register 1	0x29	00	6.2
General-purpose I/O Port C Complex Function Setting Register 2	0x2A	00	6.2
General-purpose I/O Port D Complex Function Setting Register 1	0x2B	00	6.2
General-purpose I/O Port D Complex Function Setting Register 2	0x2C	00	6.2
General-purpose I/O Port E Complex Function Setting Register 1	0x2D	00	6.2
General-purpose I/O Port E Complex Function Setting Register 2	0x2E	00	6.2
General-purpose I/O Port F Complex Function Setting Register 1	0x2F	00	6.2
8052 External Interrupt 0 Control Register	0x30	00	6.3
8052 External Interrupt 1 Control Register	0x31	00	6.3
8052 External Interrupt 2 Control Register	0x32	00	6.3
8052 External Interrupt 3 Control High Bytes Register	0x33	00	6.3

Register Name	Address	Reset Default (Hex)	Index Section
8052 External Interrupt 3 Control Low Bytes Register	0x34	00	6.3
8052 External Interrupt 0 (INT0) Flag Register	0x35	00	6.3
8052 External Interrupt 1 (INT1) Flag Register	0x36	00	6.3
8052 External Interrupt 2 (INT2) Flag Register	0x37	00	6.3
8052 External Interrupt 3 (INT3) Flag High Bytes Register	0x38	00	6.3
8052 External Interrupt 3 (INT3) Flag Low Bytes Register	0x39	00	6.3
External Interrupt Request (IRQ) Control High Bytes Register	0x40	00	6.5
External Interrupt Request (IRQ) Control Low Bytes Register	0x41	00	6.5
External Interrupt Request (IRQ) Status High Bytes Register	0x42	00	6.5
External Interrupt Request (IRQ) Status Low Bytes Register	0x43	00	6.5
External Interrupt Request (IRQ) Clear High Bytes Register	0x44	00	6.5
External Interrupt Request (IRQ) Clear Low Bytes Register	0x45	00	6.5
External Interrupt Request (IRQ) Bi-directional Trigger High Bytes Register	0x46	00	6.5
External Interrupt Request (IRQ) Bi-directional Trigger Low Bytes Register	0x47	00	6.5
External Interrupt Request (IRQ) Trigger Edge High Bytes Register	0x48	00	6.5
External Interrupt Request (IRQ) Trigger Edge Low Bytes Register	0x49	00	6.5
PWM Control Register	0x50	00	6.6
PWM0 Period Control High Bytes Register	0x51	00	6.6
PWM0 Period Control Low Bytes Register	0x52	01	6.6
PWM0 Duty Cycle Control High Bytes Register	0x53	00	6.6
PWM0 Duty Cycle Control Low Bytes Register	0x54	00	6.6
PWM1 Period Control High Bytes Register	0x55	00	6.6
PWM1 Period Control Low Bytes Register	0x56	01	6.6
PWM1 Duty Cycle Control High Bytes Register	0x57	00	6.6
PWM1 Duty Cycle Control Low Bytes Register	0x58	00	6.6
PWM Control Register 1	0x5A	00	6.6
PWM Control Register 2	0x5B	00	6.6
PWM2 Period Control High Bytes Register	0x5C	00	6.6
PWM2 Period Control Low Bytes Register	0x5D	01	6.6
PWM2 Duty Cycle Control High Bytes Register	0x5E	00	6.6
PWM2 Duty Cycle Control Low Bytes Register	0x5F	00	6.6
General-purpose I/O Port A Wakeup Control Register	0x60	00	6.7
General-purpose I/O Port B Wakeup Control Register	0x61	00	6.7
General-purpose I/O Port E Wakeup Control Register	0x62	00	6.7
General-purpose I/O Port F Wakeup Control Register	0x63	00	6.7
Peripheral Interrupt Wakeup Control Register	0x64	00	6.7

Register Name	Address	Reset Default (Hex)	Index Section
General-purpose I/O Port A Wakeup Flag Register	0x65	00	6.7
General-purpose I/O Port B Wakeup Flag Register	0x66	00	6.7
General-purpose I/O Port E Wakeup Flag Register	0x67	00	6.7
General-purpose I/O Port F Wakeup Flag Register	0x68	00	6.7
Peripheral Interrupt Wakeup Flag Register	0x69	00	6.7
Wakeup Clear Register	0x6A	00	6.7
Internal Oscillator Adjust Register	0x70	40	6.8
Internal Oscillator Counter Data High Bytes Register	0x71	00	6.8
Internal Oscillator Counter Data Low Bytes Register	0x72	00	6.8
Internal Oscillator Calibration Control Register	0x73	00	6.8
Watchdog Timer Control Register	0x78	02	6.9
Watch Timer Control Register	0x7C	80	6.9
Watch Timer Output Selection Register	0x7D	00	6.9
LCD Driver Display Data Register 0	0x80	00	6.10
LCD Driver Display Data Register 1	0x81	00	6.10
LCD Driver Display Data Register 2	0x82	00	6.10
LCD Driver Display Data Register 3	0x83	00	6.10
LCD Driver Display Data Register 4	0x84	00	6.10
LCD Driver Display Data Register 5	0x85	00	6.10
LCD Driver Display Data Register 6	0x86	00	6.10
LCD Driver Display Data Register 7	0x87	00	6.10
LCD Driver Display Data Register 8	0x88	00	6.10
LCD Driver Display Data Register 9	0x89	00	6.10
LCD Driver Display Data Register 10	0x8A	00	6.10
LCD Driver Display Data Register 11	0x8B	00	6.10
LCD Driver Display Data Register 12	0x8C	00	6.10
LCD Driver Display Data Register 13	0x8D	00	6.10
LCD Driver Display Data Register 14	0x8E	00	6.10
LCD Driver Display Data Register 15	0x8F	00	6.10
LCD Driver Display Data Register 16	0x90	00	6.10
LCD Driver Display Data Register 17	0x91	00	6.10
LCD Driver Display Data Register 18	0x92	00	6.10
LCD Driver Display Data Register 19	0x93	00	6.10
LCD Driver Control Register 1	0x98	00	6.10
LCD Driver Control Register 2	0x99	00	6.10
LCD Driver Contrast Control Register	0x9A	00	6.10
LCD Driver Power-saving Control Register	0x9B	08	6.10

Register Name	Address	Reset Default (Hex)	Index Section
LCD Driver Segment Output Enable Register 1	0x9C	00	6.10
LCD Driver Segment Output Enable Register 2	0x9D	00	6.10
LCD Driver Segment Output Enable Register 3	0x9E	00	6.10
Master/Slave I^2C Control Register	0xA0	40	6.11
Master/Slave I^2C Status Register	0xA1	00	6.11
Master/Slave I^2C Transmit Buffer Register	0xA2	00	6.11
Master/Slave I^2C Transmit and Receive Buffer Register	0xA3	00	6.11
Slave I^2C Address Register	0xA4	00	6.11
Master/Slave I^2C Extended Control Register	0xA5	00	6.11
Enhanced Timer/Counter Control Register 1	0xB0	00	6.12
Enhanced Timer/Counter Control Register 2	0xB1	00	6.12
Enhanced Timer/Counter Interrupt Register	0xB2	00	6.12
Enhanced Timer/Counter Data Buffer Low Bytes Register	0xB3	00	6.12
Enhanced Timer/Counter Data Buffer High Bytes Register	0xB4	80	6.12
SPI Control Register 1	0xC0	00	6.13
SPI Control Register 2	0xC1	00	6.13
SPI Interrupt Control Register	0xC2	00	6.13
SPI Interrupt Clear Register	0xC3	00	6.13
SPI Flag Register	0xC4	00	6.13
SPI Bit Rate Setting Register	0xC5	00	6.13
SPI Transmit Buffer Register	0xC6	FF	6.13
SPI Receive Buffer Register	0xC7	00	6.13
ADC Control Register	0xD0	80	6.14
ADC Setting Control Register	0xD1	40	6.14
ADC Interrupt Control Register	0xD2	00	6.14
ADC Channel Control Register	0xD3	00	6.14
ADC Voltage Compare Data High Bytes Register	0xD4	80	6.14
ADC Voltage Compare Data Low Bytes Register	0xD5	00	6.14
ADC Converted Data High Bytes Register	0xD6	00	6.14
ADC Converted Data Low Bytes Register	0xD7	00	6.14
Comparator Control Register	0xDA	E0	6.15
Comparator Flag Register	0xDB	00	6.15
Comparator Reference Voltage Register	0xDC	00	6.15
Comparator Pin Enable Register	0xDD	00	6.15
E^2PROM Enable Register 1	0xE0	00	6.18
E^2PROM Enable Register 2	0xE1	00	6.18
E^2PROM Address Low Bytes Register	0xE2	FF	6.18

Register Name	Address	Reset Default (Hex)	Index Section
E^{2}PROM Address High Bytes Register	0xE3	0F	6.18
E^{2}PROM Control Register	0xE4	08	6.18
E^{2}PROM Data Register	0xE8	00	6.18
General-purpose I/O Port G Output Enable Control Register	0x0210	00	6.2
General-purpose I/O Port G Data Register	0x0211	00	6.2
General-purpose I/O Port G Enable Internal Pull-up Resistor Register	0x0212	3F	6.2
General-purpose I/O Port A Complex Function Setting Register 3	0x0221	00	6.2
General-purpose I/O Port B Complex Function Setting Register 3	0x0222	00	6.2
General-purpose I/O Port B Complex Function Setting Register 4	0x0223	00	6.2
General-purpose I/O Port E Complex Function Setting Register 3	0x0228	00	6.2
General-purpose I/O Port F Complex Function Setting Register 2	0x022B	00	6.2
General-purpose I/O Port G Complex Function Setting Register 1	0x022C	00	6.2
General-purpose I/O Port G Complex Function Setting Register 2	0x022D	00	6.2
PWM3 Period Control High Bytes Register	0x0250	00	6.6
PWM3 Period Control Low Bytes Register	0x0251	01	6.6
PWM3 Duty Cycle Control High Bytes Register	0x0252	00	6.6
PWM3 Duty Cycle Control Low Bytes Register	0x0253	00	6.6
PWM4 Period Control High Bytes Register	0x0254	00	6.6
PWM4 Period Control Low Bytes Register	0x0255	01	6.6
PWM4 Duty Cycle Control High Bytes Register	0x0256	00	6.6
PWM4 Duty Cycle Control Low Bytes Register	0x0257	00	6.6
PWM5 Period Control High Bytes Register	0x0258	00	6.6
PWM5 Period Control Low Bytes Register	0x0259	01	6.6
PWM5 Duty Cycle Control High Bytes Register	0x025A	00	6.6
PWM5 Duty Cycle Control Low Bytes Register	0x025B	00	6.6

6.2 I/O Port

6.2.1 Features

- ♦ 54 programmable I/O, contains: GPIOA[7:0], GPIOB[7:0], GPIOC[7:0], GPIOD[7:0], GPIOE[7:0], GPIOF[7:0], and GPIOG[5:0]
- ♦ Some I/O with special functions (such as LCD, ADC, and PWM etc.), can be configured by Special Function Register

6.2.2 Register

WT56F248/232 I/O related registers are classified into four categories:

- ♦ GPIOx_OE: Control Output/Input Register, configured to set I/O as output or input. If the corresponding bit GPIOx_OE = 1, it is an output port with 4mA driving ability
- ♦ GPIOx_D: Data Register, reading I/O data or set output of I/O
- ♦ GPIOx_PHN: Internal Pull-up resistor Enable Register. When I/O is configured as Input port (by GPIOx_OE), this register is allowed to set if I/O is with pull-up resistor. If the corresponding GPIOx_PHN bit = 0, the I/O is with internal pull-up resistor.
- ♦ GPIOx_TYP: Output mode setting Register, is configured to set I/O as Push-Pull or Open Drain type. Only GPIOA[7:0], GPIOE[7:0], or GPIOF[2:0] is allowed to set output type while others are push-pull type.

General-purpose I/O Port A Output Enable Control Register GPIOA_OE (XFR: 0x10) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_OE[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOA_OE[7:0]	General-purpose I/O Port A Output/Input setting 1: output 0: input (default)

General-purpose I/O Port B Output Enable Control Register GPIOB_OE (XFR: 0x11) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_OE[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOB_OE[7:0]	General-purpose I/O Port B Output/Input setting 1: output 0: input (default)

General-purpose I/O Port C Output Enable Control Register GPIOC_OE (XFR: 0x12) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOC_OE[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOC_OE[7:0]	General-purpose I/O Port C Output/Input setting 1: output 0: input (default)

General-purpose I/O Port D Output Enable Control Register GPIOD_OE (XFR: 0x13) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOD_OE[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOD_OE[7:0]	General-purpose I/O Port D Output/Input setting 1: output 0: input (default)

General-purpose I/O Port E Output Enable Control Register GPIOE_OE (XFR: 0x14) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOE_OE[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOE_OE[7:0]	General-purpose I/O Port E Output/Input setting 1: output 0: input (default)

General-purpose I/O Port F Output Enable Control Register GPIOF_OE (XFR: 0x15) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Name	GPIOF_OE[7:0]							

Bit Number	Bit Mnemonic	Description
7-4	GPIOF_OE[7:4]	General-purpose I/O Port F Output/Input setting 1: output 0: input (default)
3	GPIOF_OE[3]	GPIF3 is input only pin
2-0	GPIOF_OE[2:0]	General-purpose I/O Port F Output/Input setting 1: output 0: input (default)

- **: unimplemented.**

General-purpose I/O Port A Data Register GPIOA_D (XFR: 0x16) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_D[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOA_D[7:0]	General-purpose I/O Port A Output/Input data

General-purpose I/O Port B Data Register GPIOB_D (XFR: 0x17) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_D[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOB_D[7:0]	General-purpose I/O Port B Output/Input data

General-purpose I/O Port C Data Register GPIOC_D (XFR: 0x18) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOC_D[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOC_D[7:0]	General-purpose I/O Port C Output/Input data

General-purpose I/O Port D Data Register GPIOD_D (XFR: 0x19) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOD_D[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOD_D[7:0]	General-purpose I/O Port D Output/Input data

General-purpose I/O Port E Data Register GPIOE_D (XFR: 0x1A) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOE_D[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOE_D[7:0]	General-purpose I/O Port E Output/Input data

General-purpose I/O Port F Data Register GPIOF_D (XFR: 0x1B) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Name	GPIOF_D[7:0]							

Bit Number	Bit Mnemonic	Description
7-4	GPIOF_D[7:4]	General-purpose I/O Port F Output/Input data
3	GPIOF_D[3]	GPIF3 is input only pin

Bit Number	Bit Mnemonic	Description
2-0	GPIOF_D[2:0]	General-purpose I/O Port F Output/Input data

- **: unimplemented.**

General-purpose I/O Port A Enable Internal Pull-up Resistor Register GPIOA_PHN (XFR: 0x1C) Reset Value: FFh

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_PHN[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOA_PHN[7:0]	Enable General-purpose I/O Port A Pull-up Resistor setting 1: Disable Pull-up Resistor (default) 0: Enable Pull-up Resistor

General-purpose I/O Port B Enable Internal Pull-up Resistor Register GPIOB_PHN (XFR: 0x1D) Reset Value: FFh

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_PHN[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOB_PHN[7:0]	Enable General-purpose I/O Port B Pull-up Resistor setting 1: Disable Pull-up Resistor (default) 0: Enable Pull-up Resistor

General-purpose I/O Port C Enable Internal Pull-up Resistor Register GPIOC_PHN (XFR: 0x1E) Reset Value: FFh

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOC_PHN[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOC_PHN[7:0]	Enable General-purpose I/O Port C Pull-up Resistor setting 1: Disable Pull-up Resistor (default) 0: Enable Pull-up Resistor

General-purpose I/O Port D Enable Internal Pull-up Resistor Register GPIOD_PHN (XFR: 0x1F) Reset Value: FFh

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOD_PHN[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOD_PHN[7:0]	Enable General-purpose I/O Port D Pull-up Resistor setting 1: Disable Pull-up Resistor (default) 0: Enable Pull-up Resistor

General-purpose I/O Port E Enable Internal Pull-up Resistor Register GPIOE_PHN (XFR: 0x20) Reset Value: FFh

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOE_PHN[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOE_PHN[7:0]	Enable General-purpose I/O Port E Pull-up Resistor setting 1: Disable Pull-up Resistor (default) 0: Enable Pull-up Resistor

General-purpose I/O Port F Enable Internal Pull-up Resistor Register GPIOF_PHN (XFR: 0x21) Reset Value: FFh

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOF_PHN[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOF_PHN[7:0]	Enable General-purpose I/O Port F Pull-up Resister setting 1: Disable Pull-up Resistor (default) 0: Enable Pull-up Resistor

- **: unimplemented.**

General-purpose I/O Port A Output Type Control Register GPIOA_TYP (XFR: 0x22) Reset Value: FFh

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_TYP[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOA_TYP[7:0]	General-purpose I/O Port A output type setting 1: push-pull output type (default) 0: open-drain output type

General-purpose I/O Port E Output Type Control Register GPIOE_TYP (XFR: 0x23) Reset Value: FFh

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOE_TYP[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOE_TYP[7:0]	General-purpose I/O Port E output type setting 1: push-pull output type (default) 0: open-drain output type

General-purpose I/O Port F Output Type Control Register GPIOF_TYP (XFR: 0x24) Reset Value: F7h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOF_TYP[7:0]							

Bit Number	Bit Mnemonic	Description
7-4	GPIOF_TYP[7:4]	General-purpose I/O Port F output type setting 1: push-pull output type (default) 0: open-drain output type
3	GPIOF_TYP[3]	GPIF3 is input pin only with open-drain
2-0	GPIOF_TYP[2:0]	General-purpose I/O Port F output type setting 1: push-pull output type (default) 0: open-drain output type

-: unimplemented.

General-purpose I/O Port G Output Enable Control Register GPIOG_OE (XFR: 0x0210) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved		GPIOG_OE[5:0]					

Bit Number	Bit Mnemonic	Description
7-6	Reserved	
5-0	GPIOG_OE[5:0]	General-purpose I/O Port G Output/Input setting 1: output 0: input (default)

-: unimplemented.

General-purpose I/O Port G Data Register GPIOG_D (XFR: 0x0211) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved		GPIOG_D[5:0]					

Bit Number	Bit Mnemonic	Description
7-6	Reserved	
5-0	GPIOG_D[5:0]	General-purpose I/O Port G Output/Input data

-: unimplemented.

General-purpose I/O Port G Enable Internal Pull-up Resistor Register GPIOG_PHN (XFR: 0x0212) **Reset Value: 3Fh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved		GPIOG_PHN[5:0]					

Bit Number	Bit Mnemonic	Description
7-6	Reserved	-
5-0	GPIOG_PHN[5:0]	Enable General-purpose I/O Port G Pull-up Resistor setting 1: Disable Pull-up Resistor (default) 0: Enable Pull-up Resistor

-: unimplemented.

6.2.3 Port Sharing

This is used to set I/O functions, such as SPI, I²C, PWM, ADC, etc.

General-purpose I/O Port A Complex Function Setting Register1 GPIOA_FUN1 (XFR: 0x25) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	-	-	-
Name	GPA7_FUN_SLT[1:0]		GPA6_FUN_SLT[1:0]		GPA5_FUN_SLT	Reserved		

Bit Number	Bit Mnemonic	Description
7-6	GPA7_FUN_SLT[1:0]	Set GPIOA7D complex function 00: GPIO/IRQ7 (default) 01: PWM1 output of Path A 10: ETMO output 11: ADC0 input
5-4	GPA6_FUN_SLT[1:0]	Set GPIOA6D complex function 00: GPIO/IRQ6 (default) 01: PWM2 output of Path A 10: SPI STBB input pin 11: -
3	GPA5_FUN_SLT	Set GPIOA5D complex function 1: XSOUT (served as sub crystal oscillator output pin, and was forced to set GPIOA4D as sub crystal oscillator input pin (XSIN) instead of GPIO function) 0: GPIO (default), and meanwhile GPIOA4 will be set as GPIO function.
2-0	Reserved	-

-: unimplemented.

Notes: The setting of using External Sub Crystal Oscillator as SOURCE clock:

1. Set GPIOA5 and GPIOA4 as Input port. (XFR 0x10 GPIOA_OE[5:4])
2. GPIOA5 and GPIOA4 disable internal pull high resistor. If enable pull high resistor will result in oscillator outputs unstable frequency. (XFR 0x1C GPIOA_PHN[5:4])
3. Set GPIOA5 and GPIOA4 as Sub Crystal Oscillator pin. (XFR 0x25 GPA5_FUN_SLT)
4. Set the driving ability of External Crystal Oscillator. (XFR 0x01 SPEEDUP_C32K[1:0])
5. Power on External Crystal Oscillator switch. (XFR 0x07 CRY_32K_PD)
6. Switch SOURCE clock to External Crystal Oscillator. (XFR 0x05 SOURCE_CLK_SLT[1:0])

General-purpose I/O Port A Complex Function Setting Register2 GPIOA_FUN2 (XFR: 0x26) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	-	-	-	R/W	-
Name	GPA3_FUN_SLT[1:0]		GPA2_FUN_SLT	Reserved			GPA0_FUN_SLT	Reserved

Bit Number	Bit Mnemonic	Description
7-6	GPA3_FUN_SLT[1:0]	Set GPIOA3D complex function 00: GPIO/IRQ5 (default)) 01: I²C SDA data pin, and was forced to set GPIOE7DH as I²C SCL pin instead of GPIO function 10: SPI MISO data pin 11: P03 output/input (mapping to 8052 P0.3) Regarding PWM3 Output pin setting of Path A, please refer to GPA3_FUN_SLT2 (Address 0x0221) Note: when using 8052 port (P0.x), please set the corresponding GPIOx_TYP as open-drain.
5	GPA2_FUN_SLT	Set GPIOA2D complex function 1: XMIN (main crystal oscillator input pin), will auto define GPIOA1D as main crystal oscillator output pin (XMOUT) without GPIO function 0: GPIO (default)
4-2	Reserved	-
1	GPA0_FUN_SLT	Set GPIOA0D complex function 1: SPI MOSIB data pin 0: GPIO/IRQ4 (default))
0	Reserved	-

-: unimplemented.

Notes: The setting of using External Main Crystal Oscillator as SOURCE clock:

1. Set GPIOA2 and GPIOA1 as Input port. (XFR 0x10 GPIOA_OE[2:1])

2. GPIOA2 and GPIOA1 disable internal pull high resistor. If enable pull high resistor will result in oscillator outputs unstable frequency. (XFR 0x1C GPIOA_PHN[2:1])

3. Set GPIOA2 and GPIOA1 as Main Crystal Oscillator pin. (XFR 0x26 GPA2_FUN_SLT)

4. Set the driving ability of External Main Crystal Oscillator. (XFR 0x08 CRY_12M_DR[1:0])

5. Power on External Crystal Oscillator. (XFR 0x07 CRY_12M_PD)

6. Switch SOURCE clock to External Crystal Oscillator. (XFR 0x05 SOURCE_CLK_SLT[1:0])

General-purpose I/O Port B Complex Function Setting Register 1 GPIOB_FUN1 (XFR: 0x27) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPB7_FUN_SLT[1:0]		GPB6_FUN_SLT[1:0]		GPB5_FUN_SLT[1:0]		GPB4_FUN_SLT[1:0]	

Bit Number	Bit Mnemonic	Description
7-6	GPB7_FUN_SLT[1:0]	Set GPIOB7 complex function 00: GPIO (default)) 01: RX0B, Path B RX of UART0 (If RX0B is selected, GPC0_FUN_SLT will auto select TX0B, and the rest BSEG8/ADC8 will be invalid.) 10: BSEG7, LCD SEG output 11: ADC7, ADC input

Bit Number	Bit Mnemonic	Description
5-4	GPB6_FUN_SLT[1:0]	Set GPIOB6 complex function 00: GPIO (default) 01: BUZOB, Buzzer output 10: BSEG6, LCD SEG output 11: ADC6, ADC input
3-2	GPB5_FUN_SLT[1:0]	Set GPIOB5 complex function 00: GPIO/IRQ10 (default) 01: PWM0 output of Path B 10: BSEG5, LCD SEG output 11: ADC5, ADC input P05 Output/Input (mapping to 8052 P0.5) Please refer to GPB5_FUN_SLT2 (Address 0x0222) for Pin setting. Note: when using 8052 port (P0.x), please set the corresponding GPIOx_TYP as open-drain.
1-0	GPB4_FUN_SLT[1:0]	Set GPIOB4 complex function 00: GPIO (default) 01: ACOM4, LCD COM output 10: BSEG4, LCD SEG output 11: ADC4, ADC input

General-purpose I/O Port B Complex Function Setting Register2 GPIOB_FUN2 (XFR: 0x28) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPB3_FUN_SLT[1:0]		GPB2_FUN_SLT[1:0]		GPB1_FUN_SLT[1:0]		GPB0_FUN_SLT[1:0]	

Bit Number	Bit Mnemonic	Description
7-6	GPB3_FUN_SLT[1:0]	Set GPIOB3 complex function 00: GPIO (default) 01: ACOM5, LCD COM output 10: BSEG3, LCD SEG output 11: ADC3, ADC input
5-4	GPB2_FUN_SLT[1:0]	Set GPIOB2 complex function 00: GPIO (default) 01: ACOM6, LCD COM output 10: BSEG2, LCD SEG output 11: ADC2, ADC input
3-2	GPB1_FUN_SLT[1:0]	Set GPIOB1 complex function 00: GPIO/IRQ9 (default) 01: TX0A, Path A TX of UART0 (If TX0A is selected, GPB0_FUN_SLT will auto select RX0A, and the rest ACOM7/BSEG0/ADC1 will be invalid.) 10: BSEG1, LCD SEG output 11: VREF, ADC reference voltage input P04 Output/Input (mapping to 8052 P0.4) & PWM4 output of Path B Please refer to GPB1_FUN_SLT2 (Address 0x0223) for Pin setting. Note: when using 8052 port (P0.x), please set the corresponding GPIOx_TYP as open-drain.

Bit Number	Bit Mnemonic	Description
1-0	GPB0_FUN_SLT[1:0]	Set GPIOB0 complex function 00: GPIO/IRQ8 (default) 01: ACOM7, LCD COM output 10: BSEG0, LCD SEG output 11: ADC1, ADC input Note: If GPIOB1 = TX0A, the complex function of GPIOB0 will be invalid.

General-purpose I/O Port C Complex Function Setting Register1 GPIOC_FUN1 (XFR: 0x29) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPC7_FUN_SLT[1:0]		GPC6_FUN_SLT[1:0]		GPC5_FUN_SLT[1:0]		GPC4_FUN_SLT[1:0]	

Bit Number	Bit Mnemonic	Description
7-6	GPC7_FUN_SLT[1:0]	Set GPIOC7 complex function 00: GPIO (default) 01: ASEG2, LCD SEG output 10: BSEG15, LCD SEG output 11: Reserved
5-4	GPC6_FUN_SLT[1:0]	Set GPIOC6 complex function 00: GPIO (default) 01: ASEG1, LCD SEG output 10: BSEG14, LCD SEG output 11: Reserved
3-2	GPC5_FUN_SLT[1:0]	Set GPIOC5 complex function 00: GPIO (default) 01: ASEG0, LCD SEG output 10: BSEG13, LCD SEG output 11: Reserved
1-0	GPC4_FUN_SLT[1:0]	Set GPIOC4 complex function 00: GPIO (default) 01: ACOM0, LCD COM output 10: BSEG12, LCD SEG output 11: Reserved

General-purpose I/O Port C Complex Function Setting Register2 GPIOC_FUN2 (XFR: 0x2A) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPC3_FUN_SLT[1:0]		GPC2_FUN_SLT[1:0]		GPC1_FUN_SLT[1:0]		GPC0_FUN_SLT[1:0]	

Bit Number	Bit Mnemonic	Description
7-6	GPC3_FUN_SLT[1:0]	Set GPIOC3 complex function 00: GPIO (default) 01: ACOM1, LCD COM output 10: BSEG11, LCD SEG output 11: Reserved

Bit Number	Bit Mnemonic	Description
5-4	GPC2_FUN_SLT[1:0]	Set GPIOC2 complex function 00: GPIO (default) 01: ACOM2, LCD COM output 10: BSEG10, LCD SEG output 11: Reserved
3-2	GPC1_FUN_SLT[1:0]	Set GPIOC1 complex function 00: GPIO (default) 01: ACOM3, LCD COM output 10: BSEG9, LCD SEG output 11: Reserved
1-0	GPC0_FUN_SLT[1:0]	Set GPIOC0 complex function 00: GPIO (default) 01: Reserved 10: BSEG8, LCD SEG output 11: ADC8, ADC input **Note: If GPIOB7 is set as RX0B, the complex function of GPIOC0 will be invalid.**

General-purpose I/O Port D Complex Function Setting Register1 GPIOD_FUN1 (XFR: 0x2B) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPD7_FUN_SLT[1:0]		GPD6_FUN_SLT[1:0]		GPD5_FUN_SLT[1:0]		GPD4_FUN_SLT[1:0]	

Bit Number	Bit Mnemonic	Description
7-6	GPD7_FUN_SLT[1:0]	Set GPIOD7 complex function 00: GPIO (default) 01: ASEG10, LCD SEG output 10: Reserved 11: BCOM0, LCD COM output
5-4	GPD6_FUN_SLT[1:0]	Set GPIOD6 complex function 00: GPIO (default) 01: ASEG9, LCD SEG output 10: Reserved 11: BCOM1, LCD COM output
3-2	GPD5_FUN_SLT[1:0]	Set GPIOD5 complex function 00: GPIO (default) 01: ASEG8, LCD SEG output 10: Reserved 11: BCOM2, LCD COM output
1-0	GPD4_FUN_SLT[1:0]	Set GPIOD4 complex function 00: GPIO (default) 01: ASEG7, LCD SEG output 10: Reserved 11: BCOM3, LCD COM output

General-purpose I/O Port D Complex Function Setting Register2 GPIOD_FUN2 (XFR: 0x2C) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPD3_FUN_SLT[1:0]		GPD2_FUN_SLT[1:0]		GPD1_FUN_SLT[1:0]		GPD0_FUN_SLT[1:0]	

Bit Number	Bit Mnemonic	Description
7-6	GPD3_FUN_SLT[1:0]	Set GPIOD3 complex function 00: GPIO (default) 01: ASEG6, LCD SEG output 10: BSEG19, LCD SEG output 11: BCOM4, LCD COM output
5-4	GPD2_FUN_SLT[1:0]	Set GPIOD2 complex function 00: GPIO (default) 01: ASEG5, LCD SEG output 10: BSEG18, LCD SEG output 11: BCOM5, LCD COM output
3-2	GPD1_FUN_SLT[1:0]	Set GPIOD1 complex function 00: GPIO (default) 01: ASEG4, LCD SEG output 10: BSEG17, LCD SEG output 11: BCOM6, LCD COM output
1-0	GPD0_FUN_SLT[1:0]	Set GPIOD0 complex function 00: GPIO (default) 01: ASEG3, LCD SEG output 10: BSEG16, LCD SEG output 11: BCOM7, LCD COM output

General-purpose I/O Port E Complex Function Setting Register1 GPIOE_FUN1 (XFR: 0x2D) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPE7_FUN_SLT[1:0]		GPE6_FUN_SLT[1:0]		GPE5_FUN_SLT[1:0]		GPE4_FUN_SLT[1:0]	

Bit Number	Bit Mnemonic	Description
7-6	GPE7_FUN_SLT[1:0]	Set GPIOE7DH complex function 00: GPIO/IRQ0 (default) 01: ASEG18, LCD SEG output 10: SPI SCK output 11: P00 output/input (mapping to 8052 P0.0) **Note: If GPIOA3 = I^2C SDA, GPE7_FUN_SLT will auto select I^2C SCL, and the ASEG18/SCK/P00 will be invalid.** PWM1 Output of Path B Please refer to GPE7_FUN_SLT2 (Address 0x0228) for Pin setting. Note: when using 8052 port (P0.x), please set the corresponding GPIOx_TYP as open-drain.
5-4	GPE6_FUN_SLT[1:0]	Set GPIOE6DH complex function 00: GPIO/IRQ15 (default) 01: ASEG17, LCD SEG output 10: ETMI, enhanced Timer/Counter external input 11: ADC15, ADC input **Note: If GPIOE5 = RX1, the complex function of GPIOE6DH will be invalid.**
3-2	GPE5_FUN_SLT[1:0]	Set GPIOE5DH complex function 00: GPIO/IRQ14 (default) 01: ASEG16, LCD SEG output 10: UART1 RX1 input

Bit Number	Bit Mnemonic	Description
		(If RX1 is selected, GPE6_FUN_SLT will auto select TX1, and the rest ASEG17/ETMI/ADC15 will be invalid.) 11: ADC14, ADC input
1-0	GPE4_FUN_SLT[1:0]	Set GPIOE4DH complex function 00: GPIO (default) 01: ASEG15, LCD SEG output 10: Reserved 11: ADC13, ADC input

Note 1: While using 8052 port (P0.x), please set the mapping rGPIO_TYP as open drain and connect to external pull-up resistor.

Note 2: While using UART1 or I^2C, please set the mapping rGPIO_TYP as open drain and connect to external pull-up resistor.

General-purpose I/O Port E Complex Function Setting Register2 GPE_FUN2 (XFR: 0x2E) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPE3_FUN_SLT[1:0]		GPE2_FUN_SLT[1:0]		GPE1_FUN_SLT[1:0]		GPE0_FUN_SLT[1:0]	

Bit Number	Bit Mnemonic	Description
7-6	GPE3_FUN_SLT[1:0]	Set GPIOE3DH complex function 00: GPIO/IRQ13 (default) 01: ASEG14, LCD SEG output 10: BUZOC, Buzzer output 11: ADC12, ADC input
5-4	GPE2_FUN_SLT[1:0]	Set GPIOE2DH complex function 00: GPIO/IRQ12 (default) 01: ASEG13, LCD SEG output 10: PWM5 Output of Path B 11: ADC11, ADC input
3-2	GPE1_FUN_SLT[1:0]	Set GPIOE1DH complex function 00: GPIO/IRQ11 (default) 01: ASEG12, LCD SEG output 10: Reserved 11: ADC10, ADC input
1-0	GPE0_FUN_SLT[1:0]	Set GPIOE0DH complex function 00: GPIO (default) 01: ASEG11, LCD SEG output 10: Reserved 11: ADC9, ADC input

General-purpose I/O Port F Complex Function Setting Register GPF_FUN (XFR: 0x2F) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPF3_FUN_SLT	Reserved	GPF2_FUN_SLT[1:0]		GPF1_FUN_SLT[1:0]		GPF0_FUN_SLT[1:0]	

Bit Number	Bit Mnemonic	Description
7	GPF3_FUN_SLT	Set GPIF3 function 1: Reset pin (NRST) input 0: GPIO (default)
6	Reserved	-
5-4	GPF2_FUN_SLT[1:0]	Set GPIOF2DH function 00: GPIO/IRQ3 (default) 01: CMPO, comparator output 10: T2CAP/SPI STBA (Input) 11: P02 output/input PWM3 Output of Path B Please refer to GPF2_FUN_SLT2 (Address 0x022B) for Pin setting Note: When using 8052 port (P0.x), please set the corresponding GPIOx_TYP as open-drain.
3-2	GPF1_FUN_SLT[1:0]	Set GPIOF1DH function 00: GPIO/CMPN/IRQ2 (default) 01: T2 input, Timer/counter2 external clock source input 10: SPI MOSIA data pin 11: P01 output/input (mapping to 8052 P0.1) PWM2 Output of Path B Please refer to GPF1_FUN_SLT2 (Address 0x022B) for Pin setting **Note: When GPIOF1 selects CMPN function, it must be set as GPIO Input.**
1-0	GPF0_FUN_SLT[1:0]	Set GPIOF0DH function 00: GPIO/CMPP/IRQ1 (default) 01: PWM0A, PWM0 output of Path A 10: T2O output, Timer/counter2 overflow output 11: BUZOA, Buzzer output **Note: When GPIOF0 selects CMPP function, it must be set as GPIO Input.**

-: unimplemented.

General-purpose I/O Port A Complex Function Setting Register 3 GPA_FUN3 (XFR: 0x0221) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	-	-	-	-	-	-
Name	Reserved	GPA3_FUN_SLT2	Reserved					

Bit Number	Bit Mnemonic	Description
7	Reserved	-
6	GPA3_FUN_SLT2	Set GPIOA3 Complex function 1: PWM3 Output pin of Path A 0: controlled by GPA3_FUN_SLT
5-0	Reserved	-

-: unimplemented.

General-purpose I/O Port B Complex Function Setting Register 3 GPB_FUN3 (XFR: 0x0222) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	-	-
Name	Reserved				GPB5_FUN_SLT2[1:0]		Reserved	

Bit Number	Bit Mnemonic	Description
7-4	Reserved	-
3-2	GPB5_FUN_SLT2[1:0]	Set GPIOB5 Complex function 00: controlled by GPB5_FUN_SLT 01/10: reserved 11: P05 Output/Input
1-0	Reserved	-

-: unimplemented.

General-purpose I/O Port B Complex Function Setting Register 4 GPB_FUN4 (XFR: 0x0223) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	-	-
Name	Reserved				GPB1_FUN_SLT2[1:0]		Reserved	

Bit Number	Bit Mnemonic	Description
7-4	Reserved	-
3-2	GPB1_FUN_SLT2[1:0]	Set GPIOB1 Complex function 00: controlled by GPB1_FUN_SLT 01: PWM4B 10: reserved 11: P04 Output/Input Note: While using 8052 port (P0.x), please set the mapping GPIOx_TYP as open drain.
1-0	Reserved	-

-: unimplemented.

General-purpose I/O Port E Complex Function Setting Register 3 GPE_FUN3 (XFR: 0x0228) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	-	-	-	-	-	-
Name	Reserved	GPE7_FUN_SLT2	Reserved					

Bit Number	Bit Mnemonic	Description
7	Reserved	-
6	GPE7_FUN_SLT2	Set GPIOE7 Complex function 1: PWM1B 0: controlled by GPB1_FUN_SLT
5-0	Reserved	-

-: unimplemented.

General-purpose I/O Port F Complex Function Setting Register 2 GPF_FUN2 (XFR: 0x022B) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	R/W	-	R/W	-	-
Name	Reserved			GPF2_FUN_SLT2	Reserved	GPF1_FUN_SLT2		

Bit Number	Bit Mnemonic	Description
7-5	Reserved	-
4	GPF2_FUN_SLT2	Set GPIOF2 Complex function 1: PWM3B 0: controlled by GPF2_FUN_SLT
3	Reserved	-
2	GPF1_FUN_SLT2	Set GPIOF1 Complex function 1: PWM2B 0: controlled by GPF1_FUN_SLT
1-0	Reserved	-

-: unimplemented.

General-purpose I/O Port G Complex Function Setting Register 1 GPG_FUN1 (XFR: 0x022C) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved						GPG4_FUN_SLT[1:0]	

Bit Number	Bit Mnemonic	Description
7-2	Reserved	-
1-0	GPG4_FUN_SLT[1:0]	Set GPIOG4 Complex function 00: GPIO/IRQ3B (default) 01: PWM5A 10: reserved 11: P07 Output/Input Note: when using 8052 port (P0.x), please set the mapping GPIOx_TYP as open-drain.

-: unimplemented.

General-purpose I/O Port G Complex Function Setting Register 2 GPG_FUN2 (XFR: 0x022D) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	-	-	-	-	-	-
Name	GPG3_FUN_SLT[1:0]		Reserved					

Bit Number	Bit Mnemonic	Description
7-6	GPG3_FUN_SLT[1:0]	Set GPIOG3 Complex function 00: GPIO/IRQ2B (default) 01: PWM4A 10: reserved 11: P06 Output/Input Note: when using 8052 port (P0.x), please set the mapping

Bit Number	Bit Mnemonic	Description
		GPIOx_TYP as open-drain.
5-0	Reserved	-

-: unimplemented.

LCD COM pin Setting Table:

A COM:

GPIOB0 **(ACOM7)**, GPIOB2 ~ B4 **(ACOM6 ~ ACOM4)**
GPIOC1 ~ C4 **(ACOM3 ~ ACOM0)**

B COM:

GPIOD0 ~ D7 **(BCOM7 ~ BCOM0)**

ACOM	Register Setting	BCOM	Register Setting
ACOM7	0x28 of bit 1-0: GPB0_FUN_SLT[1:0] = 01	BCOM7	0x2C of bit 1-0: GPD0_FUN_SLT[1:0] = 11
ACOM6	0x28 of bit 5-4: GPB2_FUN_SLT[1:0] = 01	BCOM6	0x2C of bit 3-2: GPD1_FUN_SLT[1:0] = 11
ACOM5	0x28 of bit 7-6: GPB3_FUN_SLT[1:0] = 01	BCOM5	0x2C of bit 5-4: GPD2_FUN_SLT[1:0] = 11
ACOM4	0x27 of bit 1-0: GPB4_FUN_SLT[1:0] = 01	BCOM4	0x2C of bit 7-6: GPD3_FUN_SLT[1:0] = 11
ACOM3	0x2A of bit 3-2: GPC1_FUN_SLT[1:0] = 01	BCOM3	0x2B of bit 1-0: GPD4_FUN_SLT[1:0] = 11
ACOM2	0x2A of bit 5-4: GPC2_FUN_SLT[1:0] = 01	BCOM2	0x2B of bit 3-2: GPD5_FUN_SLT[1:0] = 11
ACOM1	0x2A of bit 7-6: GPC3_FUN_SLT[1:0] = 01	BCOM1	0x2B of bit 5-4: GPD6_FUN_SLT[1:0] = 11
ACOM0	0x29 of bit 1-0: GPC4_FUN_SLT[1:0] = 01	BCOM0	0x2B of bit 7-6: GPD7_FUN_SLT[1:0] = 11

LCD SEG pin Setting Table:

A SEG:

GPIOE7 ~ E0 **(ASEG18 ~ ASEG11)**
GPIOD7 ~ D0 **(ASEG10 ~ ASEG3)**
GPIOC7 ~ C5 **(ASEG2 ~ ASEG0)**

B SEG:

GPIOD3 ~ D0 **(BSEG19 ~ BSEG16)**
GPIOC7 ~ C0 **(BSEG15 ~ BSEG8)**
GPIOB7 ~ B0 **(BSEG7 ~ BSEG0)**

ACOM	Register Setting	BCOM	Register Setting
ASEG18	0x2D of bit 7-6: GPE7_FUN_SLT[1:0] = 01	BSEG19	0x2C of bit 7-6: GPD3_FUN_SLT[1:0] = 10
ASEG17	0x2D of bit 5-4: GPE6_FUN_SLT[1:0] = 01	BSEG18	0x2C of bit 5-4: GPD2_FUN_SLT[1:0] = 10
ASEG16	0x2D of bit 3-2: GPE5_FUN_SLT[1:0] = 01	BSEG17	0x2C of bit 3-2: GPD1_FUN_SLT[1:0] = 10
ASEG15	0x2D of bit 1-0: GPE4_FUN_SLT[1:0] = 01	BSEG16	0x2C of bit 1-0: GPD0_FUN_SLT[1:0] = 10
ASEG14	0x2E of bit 7-6: GPE3_FUN_SLT[1:0] = 01	BSEG15	0x29 of bit 7-6: GPC7_FUN_SLT[1:0] = 10
ASEG13	0x2E of bit 5-4: GPE2_FUN_SLT[1:0] = 01	BSEG14	0x29 of bit 5-4: GPC6_FUN_SLT[1:0] = 10
ASEG12	0x2E of bit 3-2: GPE1_FUN_SLT[1:0] = 01	BSEG13	0x29 of bit 3-2: GPC5_FUN_SLT[1:0] = 10
ASEG11	0x2E of bit 1-0: GPE0_FUN_SLT[1:0] = 01	BSEG12	0x29 of bit 1-0: GPC4_FUN_SLT[1:0] = 10
ASEG10	0x2B of bit 7-6: GPD7_FUN_SLT[1:0] = 01	BSEG11	0x2A of bit 7-6: GPC3_FUN_SLT[1:0] = 10
ASEG9	0x2B of bit 5-4: GPD6_FUN_SLT[1:0] = 01	BSEG10	0x2A of bit 5-4: GPC2_FUN_SLT[1:0] = 10
ASEG8	0x2B of bit 3-2: GPD5_FUN_SLT[1:0] = 01	BSEG9	0x2A of bit 3-2: GPC1_FUN_SLT[1:0] = 10
ASEG7	0x2B of bit 1-0: GPD4_FUN_SLT[1:0] = 01	BSEG8	0x2A of bit 1-0: GPC0_FUN_SLT[1:0] = 10
ASEG6	0x2C of bit 7-6: GPD3_FUN_SLT[1:0] = 01	BSEG7	0x27 of bit 7-6: GPB7_FUN_SLT[1:0] = 10
ASEG5	0x2C of bit 5-4: GPD2_FUN_SLT[1:0] = 01	BSEG6	0x27 of bit 5-4: GPB6_FUN_SLT[1:0] = 10
ASEG4	0x2C of bit 3-2: GPD1_FUN_SLT[1:0] = 01	BSEG5	0x27 of bit 3-2: GPB5_FUN_SLT[1:0] = 10
ASEG3	0x2C of bit 1-0: GPD0_FUN_SLT[1:0] = 01	BSEG4	0x27 of bit 1-0: GPB4_FUN_SLT[1:0] = 10
ASEG2	0x29 of bit 7-6: GPC7_FUN_SLT[1:0] = 01	BSEG3	0x28 of bit 7-6: GPB3_FUN_SLT[1:0] = 10
ASEG1	0x29 of bit 5-4: GPC6_FUN_SLT[1:0] = 01	BSEG2	0x28 of bit 5-4: GPB2_FUN_SLT[1:0] = 10
ASEG0	0x29 of bit 3-2: GPC5_FUN_SLT[1:0] = 01	BSEG1	0x28 of bit 3-2: GPB1_FUN_SLT[1:0] = 10
		BSEG0	0x28 of bit 1-0: GPB0_FUN_SLT[1:0] = 10

ADC Complex Function Setting Table:

ADC	Register Setting	Shared with GPIO
ADC15	GPE6_FUN_SLT[1:0] = 11	GPIOE6
ADC14	GPE5_FUN_SLT[1:0] = 11	GPIOE5
ADC13	GPE4_FUN_SLT[1:0] = 11	GPIOE4
ADC12	GPE3_FUN_SLT[1:0] = 11	GPIOE3
ADC11	GPE2_FUN_SLT[1:0] = 11	GPIOE2
ADC10	GPE1_FUN_SLT[1:0] = 11	GPIOE1
ADC9	GPE0_FUN_SLT[1:0] = 11	GPIOE0
ADC8	GPC0_FUN_SLT[1:0] = 11	GPIOC0
ADC7	GPB7_FUN_SLT[1:0] = 11	GPIOB7
ADC6	GPB6_FUN_SLT[1:0] = 11	GPIOB6
ADC5	GPB5_FUN_SLT[1:0] = 11	GPIOB5
ADC4	GPB4_FUN_SLT[1:0] = 11	GPIOB4
ADC3	GPB3_FUN_SLT[1:0] = 11	GPIOB3
ADC2	GPB2_FUN_SLT[1:0] = 11	GPIOB2
ADC1	GPB0_FUN_SLT[1:0] = 11	GPIOB0
ADC0	GPA7_FUN_SLT[1:0] = 11	GPIOA7

ADC VREF Complex Function Setting Table:

ADC VREF	Register Setting	Shared with GPIO
VREF	GPB1_FUN_SLT[1:0] = 11	GPIOB1

Crystal Oscillator Complex Function Setting Table:

CLKIO	Register Setting	Shared with GPIO
XMOUT	GPA2_FUN_SLT = 1	GPIOA1
XMIN	GPA2_FUN_SLT = 1	GPIOA2
XSOUT	GPA5_FUN_SLT = 1	GPIOA5
XSIN	GPA5_FUN_SLT = 1	GPIOA4

SPI Complex Function Setting Table:

SPI	Register Setting	Shared with GPIO
SCK	GPE7_FUN_SLT[1:0] = 10	GPIOE7
MOSIA	GPF1_FUN_SLT[1:0] = 10	GPIOF1
MOSIB	GPA0_FUN_SLT = 1	GPIOA0
MISO	GPA3_FUN_SLT[1:0] = 10	GPIOA3
STBA	GPF2_FUN_SLT[1:0] = 10	GPIOF2
STBB	GPA6_FUN_SLT = 1	GPIOA6

UART Complex Function Setting Table:

UART	Register Setting	Shared with GPIO
RX0A	GPB1_FUN_SLT[1:0] = 01	GPIOB0
TX0A	GPB1_FUN_SLT[1:0] = 01	GPIOB1
RX0B	GPB7_FUN_SLT[1:0] = 01	GPIOB7
TX0B	GPB7_FUN_SLT[1:0] = 01	GPIOC0
RX1	GPE5_FUN_SLT[1:0] = 10	GPIOE5
TX1	GPE5_FUN_SLT[1:0] = 10	GPIOE6

Notes:

If GPIOB7 = RX0B, the complex function of GPIOC0 will be invalid, and auto define GPIOC0 as TX0B.
If GPIOB1 = TX0A, the complex function of GPIOB0 will be invalid, and auto define GPIOB0 as RX0A.

I²C Complex Function Setting Table:

I²C	Register Setting	Shared with GPIO
SDA	GPA3_FUN_SLT[1:0] = 01	GPIOA3
SCL	GPA3_FUN_SLT[1:0] = 01	GPIOE7

Comparator Complex Function Setting Table:

ACOM	Register Setting	Shared with GPIO
COMPP	Set GPIOF0 as input port	GPIOF0
COMPN	Set GPIOF1 as input port	GPIOF1
COMPO	GPF2_FUN_SLT[1:0] = 01	GPIOF2

Timer2 Pin Setting Table:

Timer2	Register Setting	Shared with GPIO
T2O	GPF0_FUN_SLT[1:0] = 10	GPIOF0
T2	GPF1_FUN_SLT[1:0] = 01	GPIOF1
T2CAP	GPF2_FUN_SLT[1:0] = 10	GPIOF2

PWM Complex Function Setting Table:

PWM	Register Setting	Shared with GPIO
PWM0A	GPF0_FUN_SLT[1:0] = 01	GPIOF0
PWM0B	GPB5_FUN_SLT[1:0] = 01	GPIOB5
PWM1A	GPA7_FUN_SLT[1:0] = 01	GPIOA7
PWM1B	GPE7_FUN_SLT2 = 1	GPIOE7
PWM2A	GPA6_FUN_SLT[1:0] = 01	GPIOA6
PWM2B	GPF1_FUN_SLT2 = 1	GPIOF1
PWM3A	GPA3_FUN_SLT2 = 1	GPIOA3
PWM3B	GPF2_FUN_SLT = 1	GPIOF2
PWM4A	GPG3_FUN_SLT[1:0] = 01	GPIOG3
PWM4B	GPB1_FUN_SLT2[1:0] = 01	GPIOB1
PWM5A	GPG4_FUN_SLT = 1	GPIOG4
PWM5B	GPE2_FUN_SLT[1:0] = 10	GPIOE2

Buzzer Complex Function Setting Table:

BUZZER	Register Setting	Shared with GPIO
BUZOA	GPF0_FUN_SLT[1:0] = 11	GPIOF0
BUZOB	GPB6_FUN_SLT[1:0] = 01	GPIOB6
BUZOC	GPE3_FUN_SLT[1:0] = 10	GPIOE3

6.3 Interrupt

The WT56F248/232 provides total nine 8052 Interrupt sources: four 8052 External Interrupts (INT0, INT1, INT2, INT3), three Timer/Counter Interrupts (TF0, TF1, TF2), and two UART Interrupts (RI0/TI0, RI1/TI1).

Each of these interrupt sources has its own enable control bit, and can be individually enabled or disabled by setting or clearing the corresponding bit in the Special Function Register IE0 or XICON.

When an interrupt is generated, CPU will jump to interrupt vector from service routine as listed below. If multiple requests of different priority levels are received simultaneously, the request of higher priority level is serviced, and then returned to service routine through RETI instruction. If interrupt flag bit is set, CPU will enter the Interrupt processing again.

Interrupt Vector Table of 8052 & Priority Level Structure:

Keil C Interrupt Number	Interrupt sources	Vector Address	Priority Level (default)	Interrupt Enable Register
0	8052 external interrupt 0	03H	1	IE.0 (EX0)
1	Timer/Counter 0 interrupt	0BH	2	IE.1 (ET0)
2	8052 external interrupt 1	13H	3	IE.2 (EX1)
3	Timer/Counter 1 interrupt	1BH	4	IE.3 (ET1)
4	Serial port 0 interrupt (UART0)	23H	5	IE.4 (ES)
5	Timer/Counter 2 interrupt	2BH	6	IE.5 (ET2)
6	Serial port 1 interrupt (UART1)	33H	7	IE.6 (ES1)
7	8052 external interrupt 2	3BH	8	XICON.2 (EX2)
8	8052 external interrupt 3	43H	9	XICON.6 (EX3)

Interrupt Enable register 0

IE0 (8052 interrupt enable register, including INT0/INT1) Address: A8H **Reset value: 00h**

7	6	5	4	3	2	1	0
EA	ES1	ET2	ES	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	1: Enable all interrupt function 0: Disable all interrupt function
6	ES1	1: Enable UART 1 interrupt 0: Disable UART 1 interrupt
5	ET2	1: Enable Timer/Counter 2 interrupt 0: Disable Timer/Counter 2 interrupt
4	ES	1: Enable UART 0 interrupt 0: Disable UART 0 interrupt
3	ET1	1: Enable Timer/Counter 1 interrupt 0: Disable Timer/Counter 1 interrupt
2	EX1	1: Enable 8052 external interrupt 1 interrupt 0: Disable 8052 external interrupt 1 interrupt
1	ET0	1: Enable Timer/Counter0 interrupt 0: Disable Timer/Counter0 interrupt
0	EX0	1: Enable 8052 external interrupt 0 interrupt 0: Disable 8052 external interrupt 0 interrupt

Interrupt Enable register 1

XICON (8052 INT2/INT3 interrupt enable register) Address: C0H **Reset value: 00h**

7	6	5	4	3	2	1	0
PX3	EX3	IE3	-	PX2	EX2	IE2	-

Bit Number	Bit Mnemonic	Description
7	PX3	Define the interrupt priority of external interrupt 3 1: INT3 has the higher priority 0: INT3 has no higher priority
6	EX3	1: Enable external interrupt 3 interrupt 0: Disable external interrupt 3 interrupt
5	IE3	If CPU detects external interrupt 3 interrupt, IE3 will be cleared by hardware. 1: has external interrupt 3 request 0: no external interrupt 3 request
4	Reserved	-
3	PX2	Define the interrupt priority of external interrupt 2 1: INT2 has the higher priority 0: INT2 has no higher priority
2	EX2	1: Enable external interrupt 2 interrupt 0: Disable external interrupt 2 interrupt
1	IE2	If CPU detects external interrupt 2 interrupt, IE2 will be cleared by hardware. 1: has external interrupt 2 request 0: no external interrupt 2 request
0	Reserved	-

- **: unimplemented**

Interrupt priority register

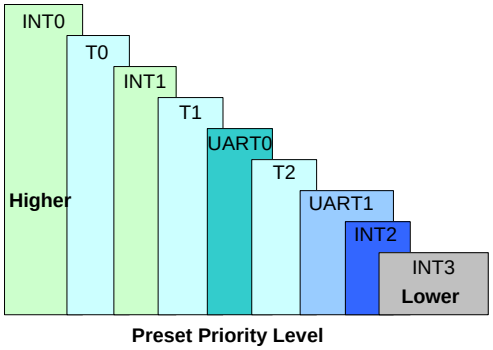
IP (8052 interrupt priority register) Address: B8H **Reset value: 00h**

7	6	5	4	3	2	1	0
-	PS1	PT2	PS	PT1	PX1	PT0	PX0

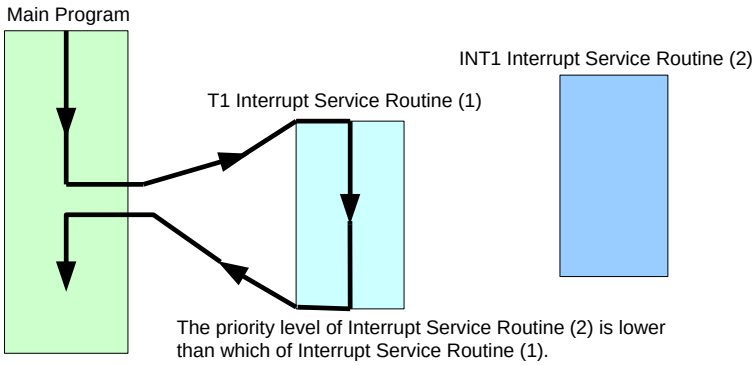
Bit number	Bit Mnemonic	Description
7	Reserved	-
6	PS1	Define the interrupt priority of UART 1 1: has the higher priority 0: has no higher priority
5	PT2	Define the interrupt priority of Timer/Counter 2 1: has the higher priority 0: has the lower priority
4	PS	Define the interrupt priority of UART 0 1: has the higher priority 0: has no higher priority
3	PT1	Define the interrupt priority of Timer/Counter 1 1: has the higher priority 0: has the lower priority
2	PX1	Define the interrupt priority of external interrupt 1 1: has the higher priority 0: has the lower priority
1	PT0	Define the interrupt priority of Timer/Counter 0 1: has the higher priority 0: has the lower priority
0	PX0	Define the interrupt priority of external interrupt 0 1: has the higher priority 0: has the lower priority

-: unimplemented

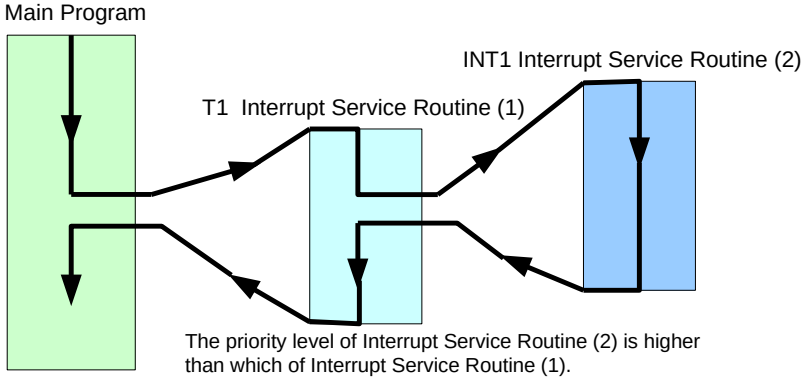
As illustrated below, if not set the priority level in Interrupt Priority Register (IP), the priority level of interrupt will be: **INT0 > T0 > INT1 > T1 > UART0 > T2 > UART1 > INT2 > INT3.**



If the higher priority is assigned to any one of the interrupts, such as set PT1 = 1, then the priority level will be:
T1 > INT0 > T0 > INT1 > UART0 > T2 > UART1 > INT2 > INT3.



If PT1 = 1 and PX1 = 1, then the priority level will be: **INT1 > T1 > INT0 > T0 > UART0 > T2 > UART1 > INT2 > INT3**, and so on. The figure below illustrated the executing procedures under different priority levels.

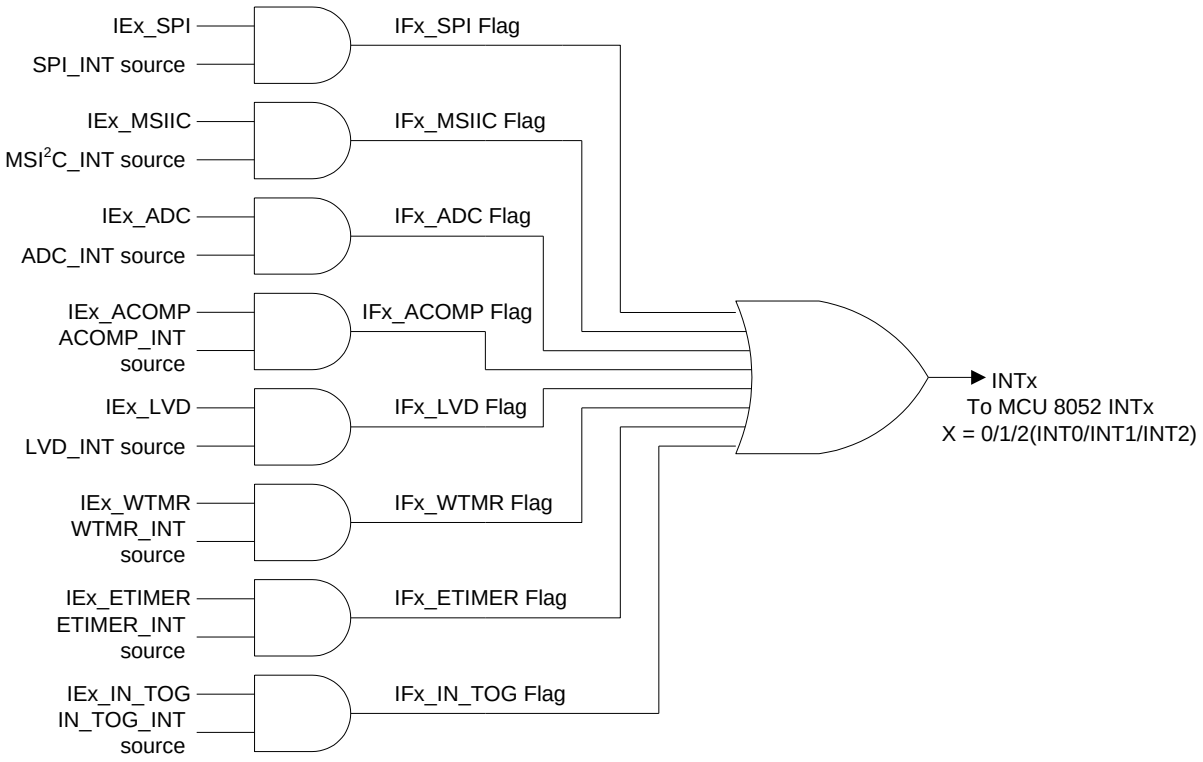


6.3.1 8052 External Interrupt 0/1/2

The WT56F248/232 supports eight peripheral interrupt sources which are derived from 8052 external interrupt 0/1/2, as described below.

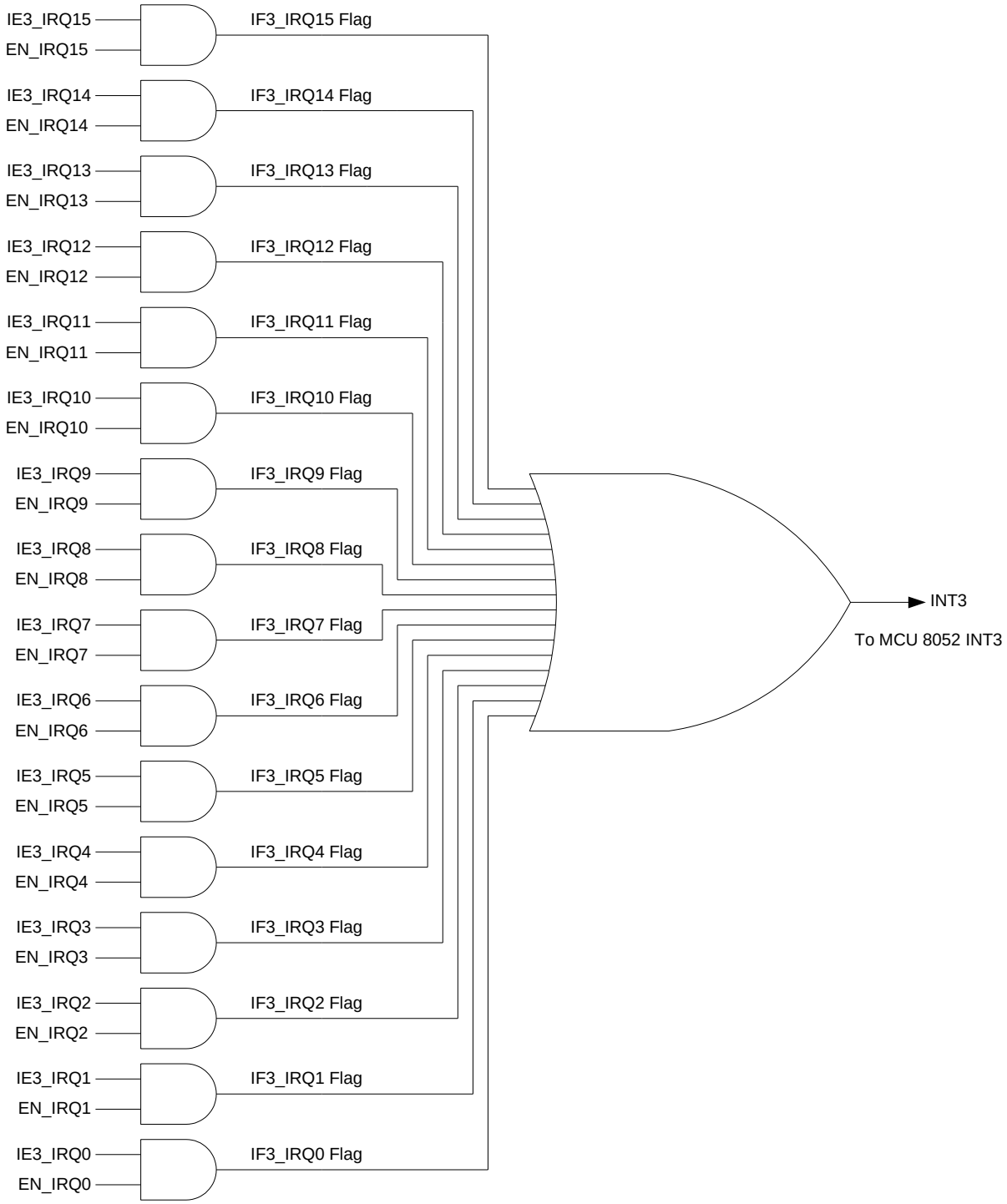
1. SPI interrupt
2. I^2C interrupt
3. ADC interrupt
4. Comparator (ACOMP) interrupt
5. Low Voltage Detection (LVD) interrupt
6. Watch Timer interrupt
7. Enhanced Timer/Counter interrupt
8. General-purpose I/O port input triggered interrupt

The figure below shows the interrupt sources of 8052 external interrupt 0/1/2:



6.3.2 8052 External Interrupt 3

WT56F248/232 contains 16 External Interrupt Request input pins. An interrupt is generated by using 8052 External Interrupt Vector 3, as illustrated below (refer to section 6.5 for more details).



8052 External Interrupt 0 Control Register IE0_CTL (XFR: 0x30) **Reset value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IE0_SPI	IE0_MSI^{2}C	IE0_ADC	IE0_ACOMP	IE0_LVD	IE0_WTMR	IE0_ETIMER	IE0_IN_TOG

Bit Number	Bit Mnemonic	Description
7	IE0_SPI	1: Enable SPI Interrupt generated by INT0 0: Disable SPI Interrupt generated by INT0
6	IE0_MSI^{2}C	1: Enable M/S I^{2}C Interrupt generated by INT0 0: Disable M/S I^{2}C Interrupt generated by INT0
5	IE0_ADC	1: Enable ADC Interrupt generated by INT0 0: Disable ADC Interrupt generated by INT0
4	IE0_ACOMP	1: Enable ACOMP Interrupt generated by INT0 0: Disable ACOMP Interrupt generated by INT0
3	IE0_LVD	1: Enable LVD Interrupt generated by INT0 0: Disable LVD Interrupt generated by INT0
2	IE0_WTMR	1: Enable Watch Timer Interrupt generated by INT0 0: Disable Watch Timer Interrupt generated by INT0
1	IE0_ETIMER	1: Enable Enhanced Timer Interrupt generated by INT0 0: Disable Enhanced Timer Interrupt generated by INT0
0	IE0_IN_TOG	1: Enable All-Input Toggle Interrupt generated by INT0 0: Disable All-Input Toggle Interrupt generated by INT0

8052 External Interrupt 1 Control Register IE1_CTL (XFR: 0x31) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IE1_SPI	IE1_MSI^{2}C	IE1_ADC	IE1_ACOMP	IE1_LVD	IE1_WTMR	IE1_ETIMER	IE1_IN_TOG

Bit Number	Bit Mnemonic	Description
7	IE1_SPI	1: Enable SPI Interrupt generated by INT1 0: Disable SPI Interrupt generated by INT1
6	IE1_MSI^{2}C	1: Enable M/S I^{2}C Interrupt generated by INT1 0: Disable M/S I^{2}C Interrupt generated by INT1
5	IE1_ADC	1: Enable ADC Interrupt generated by INT1 0: Disable ADC Interrupt generated by INT1
4	IE1_ACOMP	1: Enable ACOMP Interrupt generated by INT1 0: Disable ACOMP Interrupt generated by INT1
3	IE1_LVD	1: Enable LVD Interrupt generated by INT1 0: Disable LVD Interrupt generated by INT1
2	IE1_WTMR	1: Enable Watch Timer Interrupt generated by INT1 0: Disable Watch Timer Interrupt generated by INT1
1	IE1_ETIMER	1: Enable Enhanced Timer Interrupt generated by INT1 0: Disable Enhanced Timer Interrupt generated by INT1
0	IE1_IN_TOG	1: Enable All-Input Toggle Interrupt generated by INT1 0: Disable All-Input Toggle Interrupt generated by INT1

8052 External Interrupt 2 Control Register IE2_CTL (XFR: 0x32) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IE2_SPI	IE2_MS I^2C	IE2_ADC	IE2_ACOMP	IE2_LVD	IE2_WTMR	IE2_ETIMER	IE2_IN_TOG

Bit Number	Bit Mnemonic	Description
7	IE2_SPI	1: Enable SPI Interrupt generated by INT2 0: Disable SPI Interrupt generated by INT2
6	IE2_MSI^{2}C	1: Enable M/S I^2C Interrupt generated by INT2 0: Disable M/S I^2C Interrupt generated by INT2
5	IE2_ADC	1: Enable ADC Interrupt generated by INT2 0: Disable ADC Interrupt generated by INT2
4	IE2_ACOMP	1: Enable ACOMP Interrupt generated by INT2 0: Disable ACOMP Interrupt generated by INT2
3	IE2_LVD	1: Enable LVD Interrupt generated by INT2 0: Disable LVD Interrupt generated by INT2
2	IE2_WTMR	1: Enable Watch Timer Interrupt generated by INT2 0: Disable Watch Timer Interrupt generated by INT2
1	IE2_ETIMER	1: Enable Enhanced Timer Interrupt generated by INT2 0: Disable Enhanced Timer Interrupt generated by INT2
0	IE2_IN_TOG	1: Enable All-Input Toggle Interrupt generated by INT2 0: Disable All-Input Toggle Interrupt generated by INT2

8052 External Interrupt 3 Control High Bytes Register INT3_IRQ [15:8] (XFR: 0x33) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IE3_IRQ[15:8]							

Bit Number	Bit Mnemonic	Description
7	IE3_IRQ15	1: Enable IRQ15 Interrupt generated by INT3 0: Disable IRQ15 Interrupt generated by INT3
6	IE3_IRQ14	1: Enable IRQ14 Interrupt generated by INT3 0: Disable IRQ14 Interrupt generated by INT3
5	IE3_IRQ13	1: Enable IRQ13 Interrupt generated by INT3 0: Disable IRQ13 Interrupt generated by INT3
4	IE3_IRQ12	1: Enable IRQ12 Interrupt generated by INT3 0: Disable IRQ12 Interrupt generated by INT3
3	IE3_IRQ11	1: Enable IRQ11 Interrupt generated by INT3 0: Disable IRQ11 Interrupt generated by INT3
2	IE3_IRQ10	1: Enable IRQ10 Interrupt generated by INT3 0: Disable IRQ10 Interrupt generated by INT3
1	IE3_IRQ9	1: Enable IRQ9 Interrupt generated by INT3 0: Disable IRQ9 Interrupt generated by INT3
0	IE3_IRQ8	1: Enable IRQ8 Interrupt generated by INT3 0: Disable IRQ8 Interrupt generated by INT3

8052 External Interrupt 3 Control Low Bytes Register INT3_IRQ [7:0] (XFR: 0x34) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IE3_IRQ[7:0]							

Bit Number	Bit Mnemonic	Description
7	IE3_IRQ7	1: Enable IRQ7 Interrupt generated by INT3 0: Disable IRQ7 Interrupt generated by INT3
6	IE3_IRQ6	1: Enable IRQ6 Interrupt generated by INT3 0: Disable IRQ6 Interrupt generated by INT3
5	IE3_IRQ5	1: Enable IRQ5 Interrupt generated by INT3 0: Disable IRQ5 Interrupt generated by INT3
4	IE3_IRQ4	1: Enable IRQ4 Interrupt generated by INT3 0: Disable IRQ4 Interrupt generated by INT3
3	IE3_IRQ3	1: Enable IRQ3 Interrupt generated by INT3 0: Disable IRQ3 Interrupt generated by INT3
2	IE3_IRQ2	1: Enable IRQ2 Interrupt generated by INT3 0: Disable IRQ2 Interrupt generated by INT3
1	IE3_IRQ1	1: Enable IRQ1 Interrupt generated by INT3 0: Disable IRQ1 Interrupt generated by INT3
0	IE3_IRQ0	1: Enable IRQ0 Interrupt generated by INT3 0: Disable IRQ0 Interrupt generated by INT3

8052 External Interrupt 0 (INT0) Flag Register IF0_FLAG (XFR: 0x35) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	IF0_SPI	IF0_MSI^{2}C	IF0_ADC	IF0_ACOMP	IF0_LVD	IF0_WTMR	IF0_ETIMER	IF0_IN_TOG

Bit Number	Bit Mnemonic	Description
7	IF0_SPI	1: SPI Interrupt Event Flag be set, SPI Interrupt Flag Clear, refer to section 6.13 XFR[0xC3]
6	IF0_MSI^{2}C	1: M/S I^{2}C Interrupt Event Flag be set, M/S I^{2}C Interrupt Flag Clear, refer to section 6.11 XFR[0xA0]
5	IF0_ADC	1: ADC Interrupt Event Flag be set, will be cleared automatically after ADC conversion
4	IF0_ACOMP	1: ACOMP Interrupt Event Flag be set, ACOMP Interrupt Flag Clear, refer to section 6.15 XFR[0xDB]
3	IF0_LVD	1: LVD Interrupt Event Flag be set, LVD Interrupt Flag Clear, refer to section 6.17 XFR[0x03]
2	IF0_WTMR	1: Watch Timer Interrupt Event Flag be set, Watch Timer Interrupt Flag Clear, refer to section 6.9 XFR[0x7C]
1	IF0_ETIMER	1: Enhanced Timer Interrupt Event Flag be set, Enhanced Timer Interrupt Flag Clear, refer to section 6.12 XFR[0xB2]
0	IF0_IN_TOG	1: All-Input Toggle Interrupt Event Flag be set, Input Toggle Interrupt Clear, refer to section 6.7 XFR[0x6A]

8052 External Interrupt 1 (INT1) Flag Register IF1_FLAG (XFR: 0x36) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	IF1_SPI	IF1_MSI^{2}C	IF1_ADC	IF1_ACOMP	IF1_LVD	IF1_WTMR	IF1_ETIMER	IF1_IN_TOG

Bit Number	Bit Mnemonic	Description
7	IF1_SPI	1: SPI Interrupt Event Flag be set, SPI Interrupt Flag Clear, refer to section 6.13 XFR[0xC3]
6	IF1_MSI^{2}C	1: M/S I^{2}C Interrupt Event Flag be set, M/S I^{2}C Interrupt Flag Clear, refer to section 6.11 XFR[0xA0]
5	IF1_ADC	1: ADC Interrupt Event Flag be set, will be cleared automatically after ADC conversion
4	IF1_ACOMP	1: ACOMP Interrupt Event Flag be set, ACOMP Interrupt Flag Clear, refer to section 6.15 XFR[0xDB]
3	IF1_LVD	1: LVD Interrupt Event Flag be set, LVD Interrupt Flag Clear, refer to section 6.17 XFR[0x03]
2	IF1_WTMR	1: Watch Timer Interrupt Event Flag be set, Watch Timer Interrupt Flag Clear, refer to section 6.9 XFR[0x7C]
1	IF1_ETIMER	1: Enhanced Timer Interrupt Event Flag be set, Enhanced Timer Interrupt Flag Clear, refer to section 6.12 XFR[0xB2]
0	IF1_IN_TOG	1: All-Input Toggle Interrupt Event Flag be set, Input Toggle Interrupt Flag Clear, refer to section 6.7 XFR[0x6A]

8052 External Interrupt 2 (INT2) Flag Register IF2_FLAG (XFR: 0x37) **Reset Value: 00h**

Bit 7	Bit	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	Status	R	R	R	R	R	R	R
IF2_SPI	Name	IF2_MSI²C	IF2_ADC	IF2_ACOMP	IF2_LVD	IF2_WTMR	IF2_ETIMER	IF2_IN_TOG

Bit Number	Bit Mnemonic	Description
7	IF2_SPI	1: SPI Interrupt Event Flag be set, SPI Interrupt Flag Clear, refer to section 6.13 XFR[0xC3]
6	IF2_MSI^{2}C	1: M/S I^{2}C Interrupt Event Flag be set, M/S I^{2}C Interrupt Flag Clear, refer to section 6.11 XFR[0xA0]
5	IF2_ADC	1: ADC Interrupt Event Flag be set, will be cleared automatically after ADC conversion
4	IF2_ACOMP	1: ACOMP Interrupt Event Flag be set, ACOMP Interrupt Flag Clear, refer to section 6.15 XFR[0xDB]
3	IF2_LVD	1: LVD Interrupt Event Flag be set, LVD Interrupt Flag Clear, refer to section 6.17 XFR[0x03]
2	IF2_WTMR	1: Watch Timer Interrupt Event Flag be set, Watch Timer Interrupt Flag Clear, refer to section 6.9 XFR[0x7C]
1	IF2_ETIMER	1: Enhanced Timer Interrupt Event Flag be set, Enhanced Timer Interrupt Flag Clear, refer to section 6.12 XFR[0xB2]
0	IF2_IN_TOG	1: All-Input Toggle Interrupt Event Flag be set, Input Toggle Interrupt Flag Clear, refer to section 6.7 XFR[0x6A]

8052 External Interrupt 3 (INT3) Flag High Bytes Register IF3_IRQ [15:8] (XFR: 0x38) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	IF3_IRQ[15:8]							

Bit Number	Bit Mnemonic	Description
7	IF3_IRQ15	1: IRQ15 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x44]
6	IF3_IRQ14	1: IRQ14 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x44]
5	IF3_IRQ13	1: IRQ13 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x44]
4	IF3_IRQ12	1: IRQ12 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x44]
3	IF3_IRQ11	1: IRQ11 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x44]
2	IF3_IRQ10	1: IRQ10 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x44]
1	IF3_IRQ9	1: IRQ9 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x44]
0	IF3_IRQ8	1: IRQ8 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x44]

8052 External Interrupt 3 (INT3) Flag Low Bytes Register IF3_IRQ [7:0] (XFR: 0x39) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	IF3_IRQ[7:0]							

Bit Number	Bit Mnemonic	Description
7	IF3_IRQ7	1: IRQ7 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x45]
6	IF3_IRQ6	1: IRQ6 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x45]
5	IF3_IRQ5	1: IRQ5 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x45]
4	IF3_IRQ4	1: IRQ4 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x45]
3	IF3_IRQ3	1: IRQ3 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x45]
2	IF3_IRQ2	1: IRQ2 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x45]
1	IF3_IRQ1	1: IRQ1 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x45]
0	IF3_IRQ0	1: IRQ0 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x45]

6.4 Universal Asynchronous Receiver-Transmitter (UART)

The WT56F248/232 contains two Universal Asynchronous Receiver-Transmitters (UART0 and UART1).
As a standard UART of 8052, the Baud rate is selected by the Serial Baud rate Generator in SFR.
On Transmit and Receive, the SFR SBUFx uses two separate registers: a transmit buffer and a receive buffer register.
Transmitting data: Writing to SBUFx register and loads these data in serial output buffer, and starts transmitting.
Receiving data: Reading SBUFx register and reading the serial receive buffer. The serial port can transmit and receive simultaneously. It is also one byte receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register to prevent data loss.

The peripheral registers of UART:

SFR Name	Address	Description
PCON	87H	8052 power control register
SCON0	98H	UART 0, Control Register
SBUF0	99H	UART 0, Data Buffer
SBRG0H	9AH	Serial Baud rate Generator 0, high byte
SBRG0L	9BH	Serial Baud rate Generator 0, low byte
SCON1	D8H	UART 1, Control Register
SBUF1	D9H	UART 1, Data Buffer
SBRG1H	DAH	Serial Baud rate Generator 1, high byte
SBRG1L	DBH	Serial Baud rate Generator 1, low byte

UART0 Peripheral Registers

PCON (8052 Power Control Register) Address: 87H

7	6	5	4	3	2	1	0
SMOD1	SMOD2	-	-	-	-	-	-

SMOD1: UART0 dual rate bit.
SMOD2: UART1 dual rate bit.

-: unimplemented.

SBUF0 (8052 UART0 buffer) Address: 99H

7	6	5	4	3	2	1	0
SBUF0.7	SBUF0.6	SBUF0.5	SBUF0.4	SBUF0.3	SBUF0.2	SBUF0.1	SBUF0.0

The Serial Data Buffer of UART0. It is used to hold the bytes to be received or the bytes to be transmitted from UART0.

SBRG0H: Address: 9Ah

7	6	5	4	3	2	1	0
SBRG_EN	BRG_M[10]	BRG_M[9]	BRG_M[8]	BRG_M[7]	BRG_M[6]	BRG_M[5]	BRG_M[4]

Used to configure the Baud rate of UART0 and it must be accessed together with SBRG0L.

SBRG0L: Address: 9Bh

7	6	5	4	3	2	1	0
BRG_M[3]	BRG_M[2]	BRG_M[1]	BRG_M[0]	BRG_F[3]	BRG_F[2]	BRG_F[1]	BRG_F[0]

Used to configure the Baud rate of UART0 and it must be accessed together with SBRG0H.

SCON0 (8052 UART0 Control Register) Address: 98H

7	6	5	4	3	2	1	0
SM0_1	SM0_2	SM0_3	REN_0	TB8_0	RB8_0	TI_0	RI_0

Bit Number	Bit Mnemonic	Description
7-6	SM0_1, SM0_2	UART0 mode selection 00: Mode 0 01: Mode 1 10: Mode 2 11: Mode 3
5	SM0_3	Multi-processor Communication Enable bit In Mode 0, if SM0_3 = 0, the multi-processor communication function is disabled. In Mode 1, 2, or 3, if SM0_3 = 1, the multi-processor communication function is enabled.
4	REN_0	UART Receive Enable bit must be cleared by software. REN_0 = 1, receive starts. REN_0 = 0, receive stops.
3	TB8_0	The 9th transmit bit in Mode 2 or Mode 3, can be set or cleared by software.
2	RB8_0	In Mode 0, this bit is invalid. In Mode 1, this bit is Stop bit if SM0_3 = 0 In Mode 2 or 3, the 9th data bit that was received.
1	TI_0	Transmit Interrupt Flag. When an interrupt is complete, this bit will not be restored to “0”, and it must be cleared by software. In Mode 0, this bit is set by hardware at the end of the 8th bit, and meantime it can commence a TI_0 interrupt. In Mode 1, 2, or 3, this bit is set by hardware at the end of transmitting Stop bit, and meantime it can commence a TI_0 interrupt.
0	RI_0	Receive Interrupt Flag. When an interrupt is complete, this bit will not be restored to “0”, and it must be cleared by software. In Mode 0, this bit is set by hardware at the end of the 8th bit, and meantime it can commence a RI_0 interrupt. In Mode 1, 2, or 3, this bit is set by hardware at the end of transmitting Stop bit, and meantime it can commence a RI_0 interrupt.

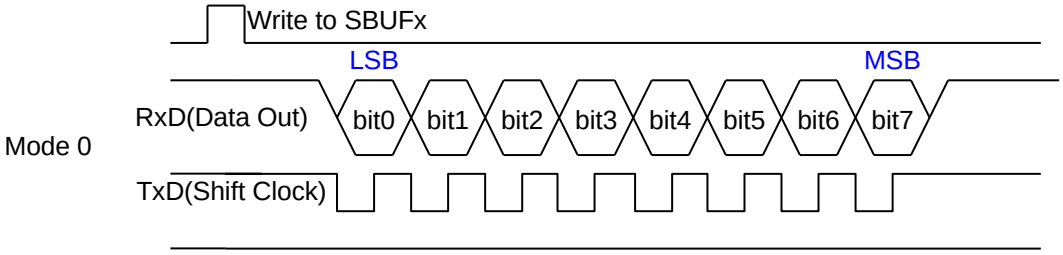
The Serial Interface 0 can operate in four modes, as described below.

SM0_1	SM0_2	Mode	Function	Baud Rate
0	0	0	Shift Register	Fosc/12
0	1	1	8-bit UART	Software programmed
1	0	2	8-bit UART	Fosc/32 or Fosc/64
1	1	3	9-bit UART	Software programmed

***Fosc = MCU clock**

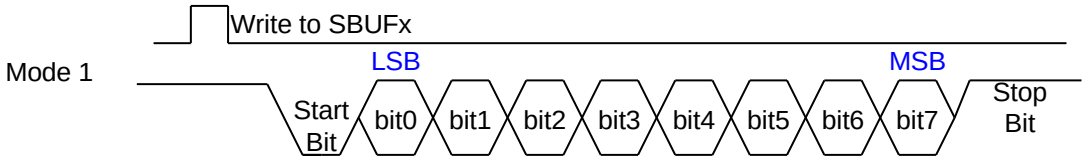
Mode 0

In Mode 0, the Baud rate of Shift transmission register is fixed at 1/12 of the oscillator frequency (*fOSC*/12). At 12 MHz, the Baud rate is 1Mbps. In this mode, no matter on receive or transmit data, Rx0 of CPUs connects each other worked as a serial data bus and Tx0 connects each other worked as a Shift pulse. On Receive, Tx0 pin sent out the shift pulse, and the serial data is received by Rx0 pin; On Transmit, it is also based on the shift pulse sent by Tx0 pin, and sent the serial data by Rx0 pin.



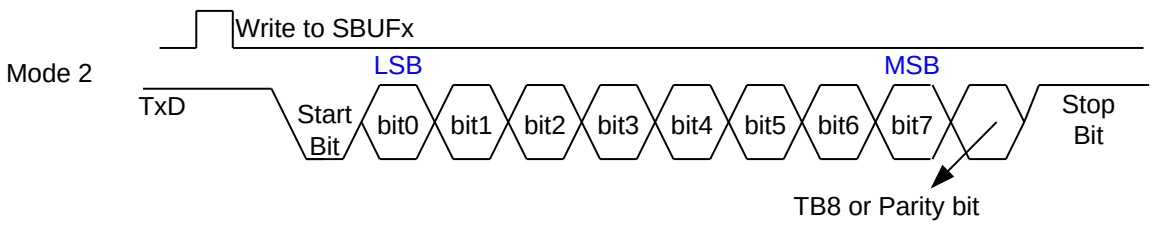
Mode 1

Mode 1 may have a variable Baud rate for serial data transmit, and the Baud rate is controlled by Timer 1.
(If UART1 is supported, Timer 2 is also available for controlling the Baud rate).
In this mode, the Rx0 pin of WT56F248/232 connects to the destination TxD pin, and the Tx0 pin of WT56F248/232 connects to the destination RxD pin.
10 bits are length of transmitted or received: a Start bit, 8 data bits, and a Stop bit. The first bit is the low level start bit (0), followed by the 8 data bits (LSB first, starts from bit 0), then the high level stop bit (1) after bit 7 (MSB).



Mode 2

Mode 2 operates at *fOSC*/32 (SMOD = 1) or *fOSC*/64 (SMOD = 0) for serial data transmission. As for the wire connection, Rx0 pin of WT56F248/232 connects to destination TxD pin and Tx0 pin of WT56F248/232 connects to destination RxD pin. 11 bits are length of transmitted or received: a Start bit, 8 data bits, a Parity bit, and 1 Stop bit. The first bit is the low level start bit (0), followed by the 8 data bits (LSB first, starts from bit 0), then the Parity bit after bit 7, and finally the high level stop bit.
On Transmit, TB8_0 in SCON0 is the 9th data bit. The TB8_0 in SCON0 will transmit the 9th data bit; On Receive, the RB8_0 in SCON0 will receive the 9th data bit.



Mode 3

The Baud rate in mode 3 is variable for serial data transmission, and it is controlled by Timer 1 (If UART1 is supported, Timer 2 is allowed to control the Baud rate). The operation in Mode 3 is the same as Mode 2.

Serial Baud rate of UART0:

SBRG_EN (SBRG0H.7)	SMOD1 (PCON.7)	Baud Rate for UART0
0	0	$\frac{1}{32}\times\frac{f_{osc}}{12\times(256-TH1)}$
0	1	$\frac{1}{16}\times\frac{f_{osc}}{12\times(256-TH1)}$
1	X	$\frac{f_{osc}}{16*(BRG\_M[10:0]+\frac{BRG\_F[3:0]}{16})}$

If SBRG_EN (SBRG0H.7) = 1,

UART0 Baud rate = $\frac{f_{osc}}{16*(BRG\_M[10:0]+\frac{BRG\_F[3:0]}{16})}$

Baud rate supporting table:

	12 MHz				
Bits/sec	**Baud Rate Register**	**BRG_M**	**BRG_F**	**Actual**	**Error**
600	1250	1250	0	600	0.0%
1200	625	625	0	1200	0.0%
2400	312.5	312	8	2400	0.0%
4800	156.25	156	4	4800	0.0%
9600	78.125	78	2	9600	0.0%
14400	52.083	52	1	14405	0.04%
19200	39.0625	39	1	19200	0.0%
38400	19.531	19	8	38461	0.16%
57600	13	13	0	57692	0.16%
115200	6.5	6	8	115384	0.16%
230400	3.25	3	4	230769	0.16%

UART1 Peripheral Register

SBUF1 (8052 UART1 buffer) Address: D9H

7	6	5	4	3	2	1	0
SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0

Serial data buffer of UART1, It is used to hold the bytes to be received or the bytes to be transmitted from UART1.

SBRG1H: Address: DAh

7	6	5	4	3	2	1	0
SBRG1_EN	BRG1_M[10]	BRG1_M[9]	BRG1_M[8]	BRG1_M[7]	BRG1_M[6]	BRG1_M[5]	BRG1_M[4]

Used to configure the Baud rate of UART1 and it must be accessed together with SBRG1L.

SBRG1L: Address: DBh

7	6	5	4	3	2	1	0
BRG1_M[3]	BRG1_M[2]	BRG1_M[1]	BRG1_M[0]	BRG1_F[3]	BRG1_F[2]	BRG1_F[1]	BRG1_F[0]

Used to configure the Baud rate of UART1 and it must be accessed together with SBRG1H.

SCON1 (8052 UART1 Control Register) Address: D8H

7	6	5	4	3	2	1	0
SM1_1	SM1_2	SM1_3	REN_1	TB8_1	RB8_1	TI_1	RI_1

UART1 Control Register

Bit Number	Bit Mnemonic	Description
7-6	SM1_1, SM1_2	UART1 mode selection 00: Mode 0 01: Mode 1 10: Mode 2 11: Mode 3
5	SM1_3	Multi-processor communication Enable bit In Mode 0, SM1_3 must be set as 0; meanwhile, the multi-processor communication function is disabled. In Mode 1, 2, and 3, if SM1_3 = 1, the multi-processor communication function is enabled.
4	REN_1	Serial Reception Enable bit. Cleared by software to disable reception. REN_1 = 1, reception starts REN_1 = 0, reception sopped
3	TB8_1	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
2	RB8_1	In Mode 0, this bit is invalid. In Mode 1, if SM1_3 = 0, this bit is Stop bit. In Mode 2 or 3, this bit is the 9th receive bit during data receiving.
1	TI_1	Transmit Interrupt Flag. When an interrupt is complete, this bit will not be resorted to “0”, and it must be cleared by software. In Mode 0, this bit is set by hardware at the end of the 8th bit time, and meantime it can commence a TI_1 interrupt.

Bit Number	Bit Mnemonic	Description
		In Mode 1, 2, or 3, this bit is set by hardware at the end of transmitting Stop bit, and meantime it can commence a TI_1 interrupt.
0	RI_1	Receive Interrupt Flag. When an interrupt is complete, this bit will not be resorted to “0”, and it must be cleared by software. In Mode 0, this bit is set by hardware at the end of the 8th bit time, and meantime it can commence a RI_0 interrupt. In Mode 1, 2, or 3, this bit is set by hardware at the end of receiving Stop bit, and meantime it can commence a RI_1 interrupt.

The Serial Interface 1 can operate in four modes, as described below.

SM1_1	SM1_2	Mode	Function	Baud Rate
0	0	0	Shift Register	Fosc/12
0	1	1	8-bit UART	Software programmed
1	0	2	8-bit UART	Fosc/32 or Fosc/64
1	1	3	9-bit UART	Software programmed

***Fosc = MCU clock**

For more information about four modes of Serial Interface 1, refer to the “**Serial Interface 0**“ content which is mentioned earlier.

Serial Baud rate of UART1:

SBRG1_EN (SBRG1H.7)	SMOD2 (PCON.6)	Baud Rate for UART1
0	0	$\frac{1}{32}\times\frac{f_{osc}}{12\times(65536-RCAP2)}$
0	1	$\frac{1}{16}\times\frac{f_{osc}}{12\times(65536-RCAP2)}$
1	X	$\frac{f_{osc}}{16*(BRG\_M[10:0]+\frac{BRG\_F[3:0]}{16})}$

If SBRG1_EN (SBRG1H.7) = 1,

UART1 Baud rate = $\frac{f_{osc}}{16*(BRG\_M[10:0]+\frac{BRG\_F[3:0]}{16})}$

Baud rate supporting table:

	12 MHz				
Bits/sec	Baud Rate Register	BRG_M	BRG_F	Actual	Error
600	1250	1250	0	600	0.0%
1200	625	625	0	1200	0.0%
2400	312.5	312	8	2400	0.0%
4800	156.25	156	4	4800	0.0%
9600	78.125	78	2	9600	0.0%
14400	52.083	52	1	14405	0.04%
19200	39.0625	39	1	19200	0.0%
38400	19.531	19	8	38461	0.16%
57600	13	13	0	57692	0.16%
115200	6.5	6	8	115384	0.16%
230400	3.25	3	4	230769	0.16%

WT56F248/232 supports two UARTs; the UART0 can select different RX0/TX0 path to prevent the pin being occupied.

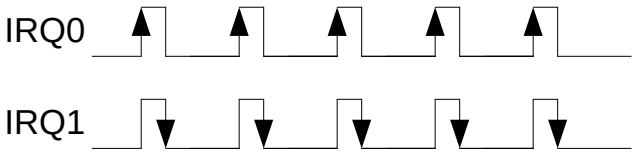
UART	**Register Setting**	**Input/output pin**
RX0A	XFR: 0x28 GPB1_FUN_SLT[1:0] = 01	GPIOB0
TX0A		GPIOB1
RX0B	XFR: 0x27 GPB7_FUN_SLT[1:0] = 10	GPIOB7
TX0B		GPIOC0
RX1	XFR: 0x2D GPE5_FUN_SLT[1:0] = 10	GPIOE5
TX1		GPIOE6

6.5 External Interrupt Request (IRQ)

- Supports 16 input Interrupts and built-in digital Filter. (The clock source of digital filer is internal oscillator 12 MHz)
- Supports single-side positive edge-triggered, negative edge-triggered, or positive edge and negative edge triggered simultaneously
- It can work with PWM, applied on motor RPM (Revolutions Per Minute) Control. PWM can generate interrupt by the corresponding IRQ, with table as below:

PWM0A/IRQ1	PWM2A/IRQ6	PWM4A/IRQ2B
PWM0B/IRQ10	PWM2B/IRQ2	PWM4B/IRQ9
PWM1A/IRQ7	PWM3A/IRQ5	PWM5A/IRQ3B
PWM1B/IRQ0	PWM3B/IRQ3	PWM5B/IRQ12

Single side triggered:



Bidirectional triggered:

External Interrupt Request (IRQ) Control High Bytes Register EN_IRQ [15:8] (XFR: 0x40) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	EN_IRQ[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	EN_IRQ[15:8]	External Interrupt Request Enable setting. Each bit is corresponded to the related IRQ pin. 1: Enable the External Interrupt Request of the corresponding pins 0: Disable the External Interrupt Request of the corresponding pins

External Interrupt Request (IRQ) Control Low Bytes Register EN_IRQ [7:0] (XFR: 0x41) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	EN_IRQ[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	EN_IRQ[7:0]	External Interrupt Request Enable setting. Each bit is corresponded to the related IRQ pin. 1: Enable the External Interrupt Request of the corresponding pins. 0: Disable the External Interrupt Request of the corresponding pins.

External Interrupt Request (IRQ) Status High Bytes Register EVT_IRQ [15:8] (XFR: 0x42) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	EVT_IRQ[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	EVT_IRQ[15:8]	External Interrupt Request Status. Each bit is corresponded to the related IRQ status. 1: an interrupt trigger occurred in the corresponding pins. 0: an interrupt trigger not occurred in the corresponding pins.

External Interrupt Request (IRQ) Status Low Bytes Register EVT_IRQ [7:0] (XFR: 0x43) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	EVT_IRQ[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	EVT_IRQ[7:0]	External Interrupt Request Status. Each bit is corresponded to the related IRQ status. 1: an interrupt trigger occurred in the corresponding pins. 0: an interrupt trigger not occurred in the corresponding pins.

External Interrupt Request (IRQ) Clear High Bytes Register CLR_IRQ [15:8] (XFR: 0x44) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	CLR_IRQ[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	CLR_IRQ[15:8]	External Interrupt Request Clear 1: writing one to the corresponding bits can clear the interrupt status 0: no action

External Interrupt Request (IRQ) Clear Low Bytes Register CLR_IRQ [7:0] (XFR: 0x45) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	CLR_IRQ[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	CLR_IRQ[7:0]	External Interrupt Request Clear 1: writing one to the corresponding bits can clear the interrupt status

Bit Number	Bit Mnemonic	Description
		0: no action

External Interrupt Request (IRQ) Bi-directional Trigger High Bytes Register IRQ_CHG [15:8] (XFR: 0x46) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IRQ_CHG[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	IRQ_CHG[15:8]	External Interrupt Request Trigger setting 1: Bi-directional triggered 0: Single-side triggered (work together with IRQ_EDGE[15:8] to set positive or negative triggered)

External Interrupt Request (IRQ) Bi-directional Trigger Low Bytes Register IRQ_CHG [7:0] (XFR: 0x47) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IRQ_CHG[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	IRQ_CHG[7:0]	External Interrupt Request Trigger setting 1: Bi-directional triggered 0: Single-side triggered (work together with IRQ_EDGE[7:0] to set positive or negative triggered)

External Interrupt Request (IRQ) Trigger Edge High Bytes Register IRQ_EDGE [15:8] (XFR: 0x48) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IRQ_EDGE[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	IRQ_EDGE[15:8]	External Interrupt Request Trigger Edge setting 1: negative edge triggered 0: positive edge triggered

External Interrupt Request (IRQ) Trigger Edge Low Bytes Register IRQ_EDGE [7:0] (XFR: 0x49) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IRQ_EDGE[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	IRQ_EDGE[7:0]	External Interrupt Request Trigger Edge setting 1: negative edge trigger 0: positive edge trigger

Note: IRQ0A/B, IRQ1A/B, IRQ2A/B, IRQ3A/B: please refer to Register 0x000B for Path selection.

6.6 Pulse Width Modulation (PWM)

WT56F248/232 provides six 16-bit precise Pulse Width Modulation modules to generate periods and Duty cycles.

- Output Frequency is 65535 levels; frequency range: 6 MHz ~ 183.1 Hz (at IRC 12 MHz)
- The resolutions of Duty and period and source clock are closely related to each other.

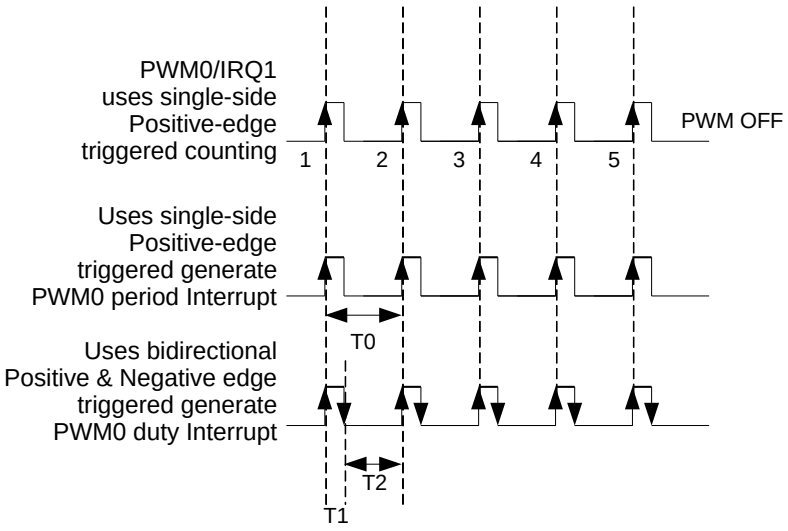
$$\text{Source clock} = 2^{\text{Duty resolution}} \times \text{Period}$$

For example, if Source clock is IRC 12 MHz, Duty Resolution is 10 bit, then the period range is limited within 11.7 kHz.

- Output type: push pull or open drain, can be configured by GPIOx_TYP[x] (GPIOF0, GPIOA7) register
- Pulse Width output will trigger external interrupt request (IRQ) to generate an interrupt, and which is used to calculate the numbers of PWM output or generate Period INT/Duty INT for Motor control application
- PWM can generate interrupt by the corresponding IRQ, with table as below:

PWM0A/IRQ1	PWM2A/IRQ6	PWM4A/IRQ2B
PWM0B/IRQ10	PWM2B/IRQ2	PWM4B/IRQ9
PWM1A/IRQ7	PWM3A/IRQ5	PWM5A/IRQ3B
PWM1B/IRQ0	PWM3B/IRQ3	PWM5B/IRQ12

For example, PWM0 outputs 5 pulses can be done by the positive-edge triggered of IRQ1, after counting for 5 times, turning off PWM0. Moreover, the period of PWM0 is able to calculate.



PWM Control Register PWM_CTL (XFR: 0x50) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	R/W	R/W	-	R/W	R/W	R/W
Name	Reserved		PWM_PLRTY[1:0]		Reserved	LBYTE_UPD_EN	PWM_EN[1:0]	

Bit Number	Bit Mnemonic	Description
7-6	Reserved	-
5	PWM_PLRTY[1:0]	1: PWM1 negative edge output 0: PWM1 positive edge output
4		1: PWM0 negative edge output 0: PWM0 positive edge output
3	Reserved	-
2	LBYTE_UPD_EN	1: Enable updating PWM output while writing PWM period or Duty Cycle Control Low Bytes Register 0: Disable updating PWM output while writing PWM period or Duty Cycle Control Low Bytes Register
1	PWM_EN[1:0]	1: Enable PWM1 function 0: Disable PWM1 function
0		1: Enable PWM0 function 0: Disable PWM0 function

-: unimplemented.

PWM0 Period Control High Bytes Register PWM0_PRD[15:8] (XFR: 0x51) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM0_PRD[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	PWM0_PRD[15:8]	PWM0_PRD[15:8] sets the output period of PWM0, and which is paired with PWM0_PRD[7:0] to form a 16-bit of period control value. PWM0 period: SOURCE clock/(PWM0_PRD[15:0]+1), source clock: 12 MHz IRC, DC ~ 24 MHz Crystal OSC. 32 kHz IRC and 32.768 kHz Crystal OSC.

PWM0 Period Control Low Bytes Register PWM0_PRD[7:0] (XFR: 0x52) **Reset Value: 01h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM0_PRD[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	PWM0_PRD[7:0]	PWM0_PRD[7:0] sets the output period of PWM0, and which is paired with PWM0_PRD[15:8] to form a 16-bit of period control value. PWM0 period: SOURCE clock/ (PWM0_PRD[15:0]+1), source clock: 12 MHz IRC, DC ~ 24 MHz Crystal OSC. 32 kHz IRC and 32.768 kHz Crystal OSC.

PWM0 Duty Cycle Control High Bytes Register PWM0_DUTY[15:8] (XFR: 0x53) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM0_DUTY[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	PWM0_DUTY[15:8]	Sets the duty cycle output of PWM0. PWM0_DUTY[15:8] sets the duty cycle of PWM0, and is paired with PWM0_DUTY[7:0] to form a 16-bit of duty cycle control value.

Note: The maximum setting of Duty must be a reasonable value.

PWM0 Duty Cycle Control Low Bytes Register PWM0_DUTY[7:0] (XFR: 0x54) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM0_DUTY[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	PWM0_DUTY[7:0]	Set the duty cycle output of PWM0 PWM0_DUTY[7:0] sets the duty cycle of PWM0, and is paired with PWM0_DUTY[15:8] to form a 16-bit of duty cycle control value.

Note: The maximum setting of Duty must be a reasonable value.

PWM1 Period Control High Bytes Register PWM1_PRD[15:8] (XFR: 0x55) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM1_PRD[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	PWM1_PRD[15:8]	PWM1_PRD[15:8] sets the output period of PWM1, and is paired with PWM1_PRD[7:0] to form a 16-bit of duty cycle control value. PWM1 period: SOURCE clock/(PWM1_PRD[15:0]+1), source clock: 12 MHz IRC, DC ~ 24 MHz Crystal OSC. 32 kHz IRC and 32.768 kHz Crystal OSC.

PWM1 Period Control Low Bytes Register PWM1_PRD[7:0] (XFR: 0x56) Reset Value: 01h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM1_PRD[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	PWM1_PRD[7:0]	PWM1_PRD[7:0] sets the output period of PWM1, and is paired with PWM1_PRD[15:8] to form a 16-bit of duty cycle control value. PWM1 period: SOURCE clock/(PWM1_PRD[15:0]+1), source clock: 12 MHz IRC, DC ~ 24 MHz Crystal OSC. 32 kHz IRC and 32.768 kHz Crystal OSC.

PWM1 Duty Cycle Control High Bytes PWM1_DUTY[15:8] (XFR: 0x57) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM1_DUTY[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	PWM1_DUTY[15:8]	Sets the duty cycle output of PWM1 PWM1_DUTY[15:8] sets the duty cycle of PWM1, and is paired with PWM1_DUTY[7:0] to form a 16-bit of duty cycle control value.

Note: The maximum setting of Duty Cycle must be a reasonable value.

PWM1 Duty Cycle Control Low Bytes Register PWM1_DUTY[7:0] (XFR: 0x58) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM1_DUTY[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	PWM1_DUTY[7:0]	Sets the duty cycle of PWM1 PWM1_DUTY[7:0] sets the duty cycle of PWM1, and is paired with PWM1_DUTY[15:8] to form a 16-bit duty cycle control value.

Note: The maximum setting of Duty Cycle must be a reasonable value.

PWM Control Register1 PWM_CTL1 (XFR: 0x5A) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				PWM_PLRTY[5:2]			

Bit Number	Bit Mnemonic	Description
7-4	Reserved	-
3	PWM_PLRTY[5:2]	1: PWM5 negative edge output 0: PWM5 positive edge output
2		1: PWM4 negative edge output 0: PWM4 positive edge output
1		1: PWM3 negative edge output 0: PWM3 positive edge output
0		1: PWM2 negative edge output 0: PWM2 positive edge output

-: unimplemented.

PWM Control Register2 PWM_CTL2 (XFR: 0x5B) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved		PWM_EN[5:0]					

Bit Number	Bit Mnemonic	Description
7-6	Reserved	-
5	PWM_EN[5:0]	1: PWM5 negative edge output 0: PWM5 positive edge output
4		1: PWM4 negative edge output 0: PWM4 positive edge output
3		1: PWM3 negative edge output 0: PWM3 positive edge output
2		1: PWM2 negative edge output 0: PWM2 positive edge output
1		1: PWM1 negative edge output 0: PWM1 positive edge output
0		1: PWM0 negative edge output 0: PWM0 positive edge output

-: unimplemented.

PWM2 Period Control High Bytes Register PWM2_PRD[15:8] (XFR: 0x5C) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM2_PRD[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	PWM2_PRD[15:8]	PWM2_PRD[15:8] sets the output period of PWM2, and which is paired with PWM2_PRD[7:0] to form a 16-bit of period control value. PWM2 period: SOURCE clock/ (PWM2_PRD[15:0]+1), source clock: 12 MHz IRC, DC ~ 24 MHz Crystal OSC. 32 kHz IRC and 32.768 kHz Crystal OSC.

PWM2 Period Control Low Bytes Register PWM2_PRD[7:0] (XFR: 0x5D) **Reset Value: 01h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM2_PRD[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	PWM2_PRD[7:0]	PWM2_PRD[7:0] sets the output period of PWM2, and which is paired with PWM2_PRD[15:8] to form a 16-bit of period control value. PWM2 period: SOURCE clock/ (PWM2_PRD[15:0]+1), source clock: 12 MHz IRC, DC ~ 24 MHz Crystal OSC. 32 kHz IRC and 32.768 kHz Crystal OSC.

PWM2 Duty Cycle Control High Bytes Register PWM2_DUTY[15:8] (XFR: 0x5E) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM2_DUTY[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	PWM2_DUTY[15:8]	PWM2_DUTY[15:8] sets the output duty cycle of PWM2, and which is paired with PWM2_DUTY[7:0] to form a 16-bit of period control value.

Note: The maximum setting of Duty Cycle must be a reasonable value.

PWM2 Duty Cycle Control Low Bytes Register PWM2_DUTY[7:0] (XFR: 0x5F) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM2_DUTY[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	PWM2_DUTY[7:0]	PWM2_DUTY[7:0] sets the output duty cycle of PWM2, and which is paired with PWM2_DUTY[15:8] to form a 16-bit of period control value.

Note: The maximum setting of Duty Cycle must be a reasonable value.

PWM3 Period Control High Bytes Register PWM3_PRD[15:8] (XFR: 0x0250) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM3_PRD[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	PWM3_PRD[15:8]	PWM3_PRD[15:8] sets the output period of PWM3, and is paired with PWM3_PRD[7:0] to form a 16-bit of duty cycle control value. PWM3 period: SOURCE clock/(PWM3_PRD[15:0]+1), source clock: 12 MHz IRC, DC ~ 24 MHz Crystal OSC. 32 kHz IRC and 32.768 kHz Crystal OSC.

PWM3 Period Control Low Bytes Register PWM3_PRD[7:0] (XFR: 0x0251) **Reset Value: 01h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM3_PRD[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	PWM3_PRD[7:0]	PWM3_PRD[7:0] sets the output period of PWM3, and is paired with PWM3_PRD[15:8] to form a 16-bit of duty cycle control value. PWM3 period: SOURCE clock/(PWM3_PRD[15:0]+1), source clock: 12 MHz IRC, DC ~ 24 MHz Crystal OSC. 32 kHz IRC and 32.768 kHz Crystal OSC.

PWM3 Duty Cycle Control High Bytes Register PWM3_DUTY[15:8] (XFR: 0x0252) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM3_DUTY[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	PWM3_DUTY[15:8]	PWM3_DUTY[15:8] sets the output duty cycle of PWM3, and which is paired with PWM3_DUTY[7:0] to form a 16-bit of period control value.

Note: The maximum setting of Duty Cycle must be a reasonable value.

PWM3 Duty Cycle Control Low Bytes Register PWM3_DUTY[7:0] (XFR: 0x0253) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM3_DUTY[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	PWM3_DUTY[7:0]	PWM3_DUTY[7:0] sets the output duty cycle of PWM3, and which is paired with PWM3_DUTY[15:8] to form a 16-bit of period control value.

Note: The maximum setting of Duty Cycle must be a reasonable value.

PWM4 Period Control High Bytes Register PWM4_PRD[15:8] (XFR: 0x0254) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM4_PRD[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	PWM4_PRD[15:8]	PWM4_PRD[15:8] sets the output period of PWM4, and is paired with PWM4_PRD[7:0] to form a 16-bit of duty cycle control value. PWM4 period: SOURCE clock/(PWM4_PRD[15:0]+1), source clock: 12 MHz IRC, DC ~ 24 MHz Crystal OSC. 32 kHz IRC and 32.768 kHz Crystal OSC.

PWM4 Period Control Low Bytes Register PWM4_PRD[7:0] (XFR: 0x0255) **Reset Value: 01h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM4_PRD[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	PWM4_PRD[7:0]	PWM4_PRD[7:0] sets the output period of PWM4, and is paired with PWM4_PRD[15:8] to form a 16-bit of duty cycle control value. PWM4 period: SOURCE clock/(PWM4_PRD[15:0]+1), source clock: 12 MHz IRC, DC ~ 24 MHz Crystal OSC. 32 kHz IRC and 32.768 kHz Crystal OSC.

PWM4 Duty Cycle Control High Bytes Register PWM4_DUTY[15:8] (XFR: 0x0256) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM4_DUTY[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	PWM4_DUTY[15:8]	PWM4_DUTY[15:8] sets the output duty cycle of PWM4, and which is paired with PWM4_DUTY[7:0] to form a 16-bit of period control value.

Note: The maximum setting of Duty Cycle must be a reasonable value.

PWM4 Duty Cycle Control Low Bytes Register PWM4_DUTY[7:0] (XFR: 0x0257) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM4_DUTY[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	PWM4_DUTY[7:0]	PWM4_DUTY[7:0] sets the output duty cycle of PWM4, and which is paired with PWM4_DUTY[15:8] to form a 16-bit of period control value.

Note: The maximum setting of Duty Cycle must be a reasonable value.

PWM5 Period Control High Bytes Register PWM5_PRD[15:8] (XFR: 0x0258) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM5_PRD[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	PWM5_PRD[15:8]	PWM5_PRD[15:8] sets the output period of PWM5, and is paired with PWM5_PRD[7:0] to form a 16-bit of duty cycle control value. PWM5 period: SOURCE clock/(PWM5_PRD[15:0]+1), source clock: 12 MHz IRC, DC ~ 24 MHz Crystal OSC. 32 kHz IRC and 32.768 kHz Crystal OSC.

PWM5 Period Control Low Bytes Register PWM5_PRD[7:0] (XFR: 0x0259) **Reset Value: 01h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM5_PRD[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	PWM5_PRD[7:0]	PWM5_PRD[7:0] sets the output period of PWM5, and is paired with PWM5_PRD[15:8] to form a 16-bit of duty cycle control value. PWM5 period: SOURCE clock/(PWM5_PRD[15:0]+1), source clock: 12 MHz IRC, DC ~ 24 MHz Crystal OSC. 32 kHz IRC and 32.768 kHz Crystal OSC.

PWM5 Duty Cycle Control High Bytes Register PWM5_DUTY[15:8] (XFR: 0x025A) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM5_DUTY[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	PWM5_DUTY[15:8]	PWM5_DUTY[15:8] sets the output duty cycle of PWM5, and which is paired with PWM5_DUTY[7:0] to form a 16-bit of period control value.

Note: The maximum setting of Duty Cycle must be a reasonable value.

PWM5 Duty Cycle Control Low Bytes Register PWM5_DUTY[7:0] (XFR: 0x025B) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM5_DUTY[7:0]							

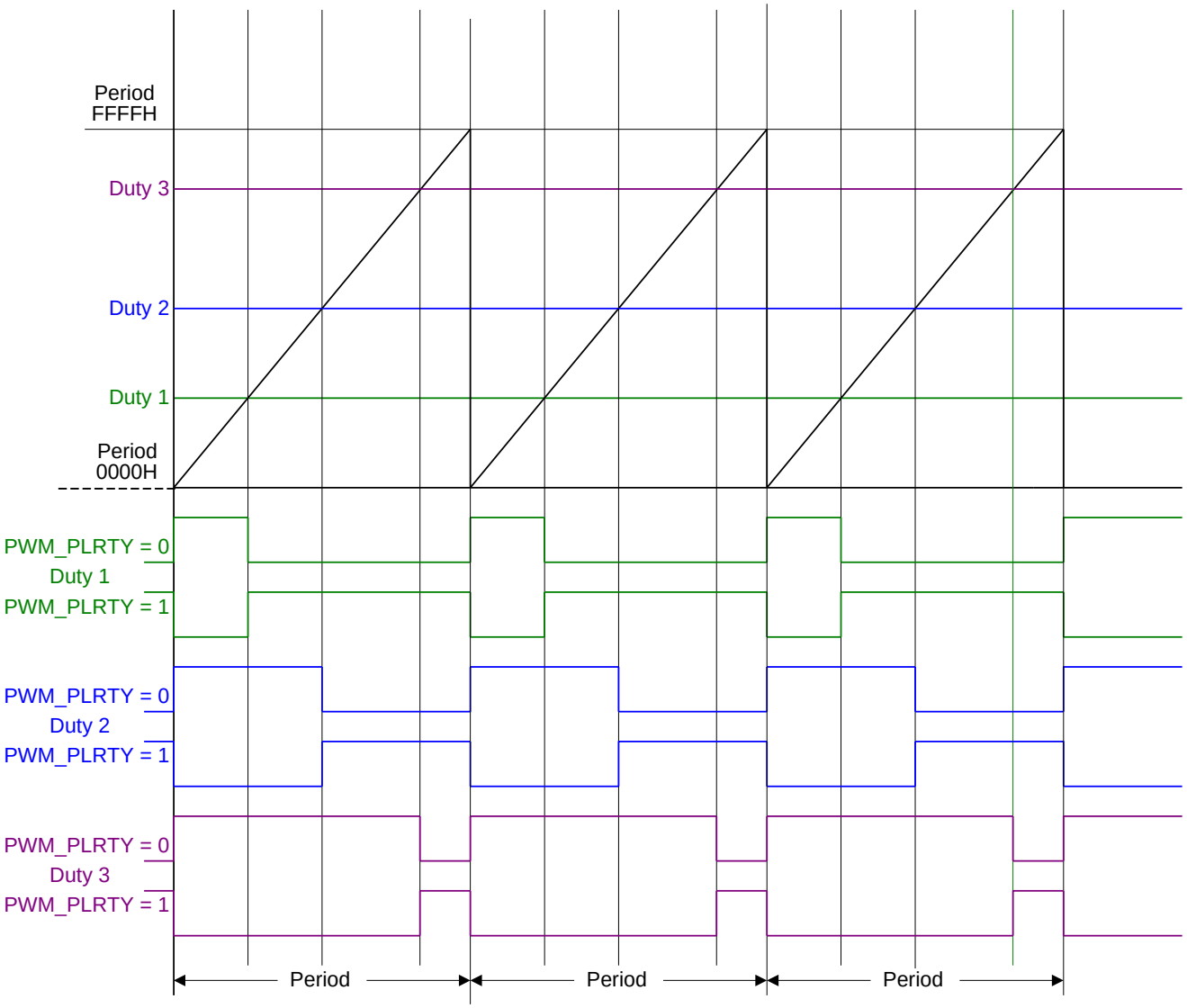
Bit Number	Bit Mnemonic	Description
7-0	PWM5_DUTY[7:0]	PWM5_DUTY[7:0] sets the output duty cycle of PWM5, and which is paired with PWM5_DUTY[15:8] to form a 16-bit of period control value.

Note: The maximum setting of Duty Cycle must be a reasonable value.

PWM0/PWM1/PWM2/PWM3/PWM4/PWM5 Period Setting example:

$$\text{Period} = \frac{\text{Source clock (if: IRC 12MHz)}}{\text{PWMx\_PRD} + 1}$$

PWMx_PRD	PWM output period
1	6 MHz (Max.)
3	3 MHz
11	1 MHz
23	500 kHz
59	200 kHz
119	100 kHz
239	50 kHz
599	20 kHz
1199	10 kHz
2399	5 kHz
2999	4 kHz
3999	3 kHz
5999	2 kHz
11999	1 kHz
23999	500 Hz
29999	400 Hz
39999	300 Hz
59999	200 Hz
65535	183.1 Hz (Min.)



6.7 Power Management

WT56F248/232 provides four operation modes, as listed below.

- Normal mode
- Green mode
- Idle mode
- Sleep mode

Four operation mode switching is illustrated in the figure below:

Operating Mode	8052	Peripheral Clock	XTAL (12 MHz)	XTAL (32.768 kHz)	IRC (12 MHz)	IRC (32 kHz)	Power Consumption@5V	Note
Normal 1	on	on	off	off	on	on	3.6 mA	*1
Normal 2	on	on	off	on	on	on	3.6 mA	*2
Normal 3	on	on	on	off	off	off	4.4 mA	*3
Green 1	on	on	off	off	off	on	17 uA	*4 *6
Green 2	on	on	off	on	off	off	40 uA	*5 *6
Idle 1	off	on	off	off	on	on	650 uA	*7 *9 *12
Idle 2	off	off	off	off	on	on	500 uA	*8 *9 *12
Sleep 1	off	off	off	off	off	off	300 uA	*10 *12
Sleep 2	off	off	off	off	off	off	5 uA	*11 *12

Notes:

1. LCD power consumption: Normal Load = 5 /480k = 10.4uA @5V; Heavy Load = 5 /240k = 20.8uA @5V

2. LVD&LVDR power consumption is about 5uA@5V

3. LVR power consumption is about 5uA@5V

4. BLDO power consumption 170uA@5V (can be turned off only on Green 1 & Green 2 modes)

***1 Normal 1 Mode: MCU all use the internal oscillator, and therefore this mode is the most cost-saving mode, but IRC 12 MHz will be affected by the impact of temperature, please refer to section 7.5.**

***2 Normal 2 Mode: use external oscillator 32.768 kHz to calibrate IRC 12 MHz, and calibration can reach ±1%.**

***3 Normal 3 Mode: this mode is focused on precise high frequency. Calendar or Clock function can only be achieved by 8052 Timer due to without external 32.768 kHz oscillator.**

***4 Green 1 Mode: After Source clock selecting internal IRC 32 kHz, manually turn off main BLDO to reduce power consumption. The frequency tolerance of internal IRC 32 kHz is ±30%.**

***5 Green 2 Mode: Prior to selecting Source clock of External Crystal Oscillator 32.768 kHz, please manually turn on the power of external crystal oscillator 32.768 kHz (CRY_32K_PD) to allow external crystal oscillator start oscillation. Due to the external crystal oscillator 32.768 kHz with small frequency tolerance, Calendar or Clock function can be achieved by Watch Timer.**

***6 Prior to switching back to Normal Mode in Green 1 & Green 2 mode, please turn on main BLDO first, then select Source clock to work at internal IRC (12/24 MHz) or external oscillator (DC~24 MHz).**

***7 Idle 1 Mode: Enable MCU_CLK_OFF to enter Idle mode, this mode wakeup fast and support the most wakeup sources, please refer to the Wakeup source illustration figure as below.**

***8 Idle 2 Mode: Enable SYSTEM_CLK_OFF to enter Idle mode, this mode turn off Peripheral Clock, thus MCU cannot use INT0/1/2_WK to wakeup, please refer to the Wakeup source illustration figure as below.**

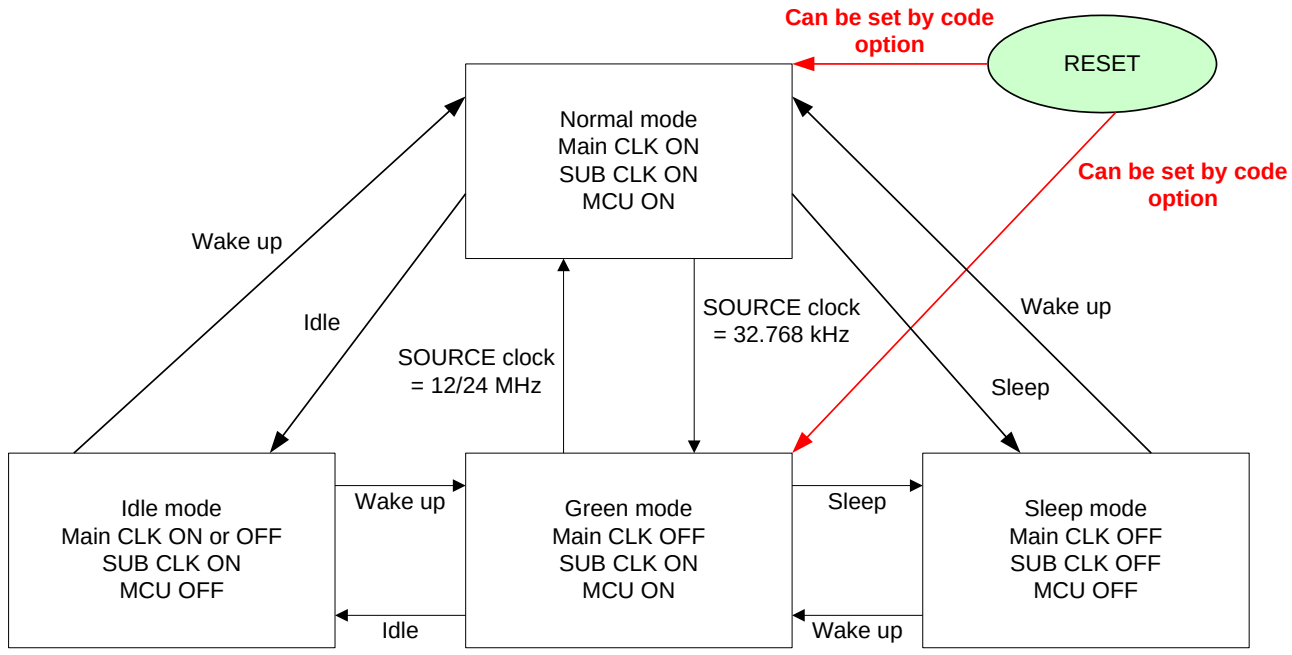
***9 Wakeup time of Idle 1 & Idle 2 Mode: 2 clocks**
If Source clock = 12 MHz, wakeup time: 2 * (1/12 MHz) = 166ns;
If Source clock = 24 MHz, wakeup time: 2 * (1/24 MHz) = 83.3ns;
If Source clock = 32 kHz, Wakeup time: 2 * (1/32 kHz) = 62.5us.

***10 Sleep 1 Mode.: This mode is about Source clock enable IRC12M_CLK_OFF at IRC 12 MHz, allowing MCU to enter Sleep mode, and support fast Wakeup. The wakeup time is 8 * (1/12 MHz) = 666ns (Sleep 1 mode only supports IRC12M). Please refer to the Wakeup source illustration figure as below.**

***11 Sleep 2 Mode.: Enable SOURCE_CLK_OFF to enter Sleep mode.**
If Source clock = IRC oscillator (in the meantime, Sleep 2 only supports IRC12M), the wakeup time is 128 clocks. 128*(1/12 MHz) = 10.66us@12 MHz;
If Source clock = External crystal oscillator, the wakeup time is 16*1024 clocks.
16*1024*(1/12 MHz) = 1360us@12 MHz or 16*1024*(1/24 MHz) = 680ns@24 MHz.
Please refer to the Wakeup source illustration figure as below.

***12 Adopts Watch Timer Wakeup in Idle & Sleep mode, turn on the External Sub crystal oscillator power (IRC_32K_PD or CRY_32K_PD) as the clock source of Watch Timer, in the meantime the power-consuming is increasing.**

MCU Operation Mode figure:



WT56F248/232 provides many sources of wakeup returning itself from sleep/idle mode to normal mode.

The figure below illustrated the Wakeup sources below each mode:

SOURCE		Idle 1	Idle 2	Sleep Mode
		MCU_CLK_OFF	SYSTEM_CLK_OFF	SOURCE_CLK_OFF IRC12M_CLK_OFF
NRST		○	○	○
GPIOx_WK[x]		○	○	○
INT0/1/2_WK	IE0/1/2_SPI	○	×	×
	IE0/1/2_MSIIC	○	×	×
	IE0/1/2_ADC	×	×	×
	IE0/1/2_ACOMP	○	×	×
	IE0/1/2_LVD	○	○	○
	IE0/1/2_WTMR	×	×	×
	IE0/1/2_ETIMER	○	×	×
	IE0/1/2_IN_TOG	○	○	○
INT3_WK	IRQ[15:0]	×	×	×
ADC_WK		○	○	○
ACOMP_WK		○	○	○
WTMR_WK		○	○	○

Notes:

1. GPIOx_WK[x] & IE0/1/2_IN_TOG: only support 28 general-purpose I/O pin Toggle (GPIO A/B/E/F).

2. IRQ[15:0]: IRQ did not support wakeup, please use GPIOx_WK[x] to wakeup.

3. ADC_WK: Based on input source for comparing Toggle wakeup

4. WTMR_WK: Turn on sub crystal oscillator (IRC 32 kHz or Ext 32 kHz) and sub crystal oscillator power to be the clock source of Watch Timer.

ISP Clock Source Control Register ISP_CHG_CTL (XFR: 0x04) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R	-	-	R	R
Name	ISP_CHG_12M	IIC_ISP_CHG	UART_ISP_CHG	ISP_CHG_FLAG	Reserved		LVD_RST_ACT_FLG	LVR_ACT_FLG

Bit Number	Bit Mnemonic	Description
7	ISP_CHG_12M	When MCU is in Green & Sleep mode, ISP pin will turn on the internal 12 MHz RC oscillator automatically 1: Enable 0: Disable
6	IIC_ISP_CHG	I^2C pin trigger ISP clock source as internal 12 MHz RC oscillator 1: Enable 0: Disable
5	UART_ISP_CHG	UART pin (GPIF3) trigger ISP clock source as internal 12 MHz RC oscillator 1: Enable 0: Disable
4	ISP_CHG_FLAG	ISP_CHG_FLAG = 1: MCU is waken up by SWUT pin. Turn on internal 12 MHz RC oscillator and SOURCE clock switch to 12 MHz. Clear ISP_CHG_FLAG by setting ISP_CHG_12M bit = 0
3-2	Reserved	-
1	LVD_RST_ACT_FLG	1 : Power Voltage ＜ Setting Low Voltage Detection Reset Range. (This flag is not connected to the Analog Filter, and will be affected easily. For reference only)
0	LVR_ACT_FLG	1 : Power Voltage ＜ Internal Low Voltage Reset Voltage. (This flag is not connected to the Analog Filter, and will be affected easily. For reference only)

-: unimplemented.

Note: If Source clock is non-12 MHz application, please add below Forcing Toggle SWUT setting procedure to the program enabling MCU programming repeatedly.

Non 12 MHz mode contains: Green, Sleep mode or use external oscillator (non 12 MHz) can enable ISP_CHG_12M & UART_ISP_CHG bit allow MCU pin trigger to switch the SOURCE clock & ISP clock to internal 12 MHz RC oscillator by SWUT, and meanwhile MCU can receive the correct ISP command.

Mandatory trigger SWUT setting procedures:
1. Program Initialized Enable ISP_CHG_12M & UART_ISP_CHG bit.
   rISP_CHG_CTL = 0xA0;
2. Program main loop judge if ISP_CHG_FLAG been triggered, and based on Sleep mode to add one software wakeup mechanism, please refer to the example program.

```
   void DRV_CheckSwutTriggerWakeup(void)
{
      //If enable rISP_CHG_CTL of bit 7 and Bit.
      //When Swut pin have hi to low(2V) level, MCU will change source clock to IRC 12 MHz
      if(rISP_CHG_CTL & 0x10)
      {
         DRV_SoftwareWakeup();
         //need delay 100ms(minimum) to wait ISP command, Don't remove this delay
command
         DelayWhile(100);          //This time MCU change source clock to IRC 12 MHz
         rISP_CHG_CTL = 0x00;    //Disable ISP change clock. MCU go back to original setting
         rISP_CHG_CTL = 0xA0;    //Enable ISP change clock
      }
}
```

Code Option setting General-purpose I/O Complex Function mapping registers, including Crystal Oscillator pins, Reset, Low Voltage Detection Reset option setting.

System Clock Source Control Register SOURCE_CLK_SLT (XFR: 0x05) **Reset Value: A0h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				SOURCE_CLK_SLT[1:0]		MCU_CLK_SLT[1:0]	

Bit Number	Bit Mnemonic	Description
7-4	-	Must be equal to “1010”, otherwise bit [3:0] cannot be written into.
3-2	SOURCE_CLK_SLT[1:0]	Select SOURCE clock sources 00: internal 12 MHz RC oscillator (default) 01: external DC ~ 24 MHz crystal oscillator 10: internal 32 kHz RC oscillator 11: external 32.768 kHz crystal oscillator Default value can be selected by section 6.19 Code Option Select
1-0	MCU_CLK_SLT[1:0]	MCU clock setting 00: MCU clock = SOURCE clock (default) 01: MCU clock = SOURCE clock /2 10: MCU clock = SOURCE clock /4 11: MCU clock = SOURCE clock /12

-: unimplemented.

Note: Before switching to SOURCE_CLK_SLT[1:0], please set the IRC_12M_PD Register and power on.

Power-saving Control Register POWER_SAVE_CTL (XFR: 0x06) **Reset Value: 50h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				MCU_CLK_OFF	SYSTEM_CLK_OFF	SOURCE_CLK_OFF	IRC12M_CLK_OFF

Bit Number	Bit Mnemonic	Description
7-4	-	Must be equal to “0101”, otherwise, Bit[3:0] cannot be written into
3	MCU_CLK_OFF	1: MCU clock is Off (including MCU and partial peripheral hardware), and MCU must wait for 3~4 MCU clock cycles until MCU clock ON and work. 0: MCU clock is On.
2	SYSTEM_CLK_OFF	1: MCU clock is Off (including MCU and partial peripheral hardware), and MCU must wait for 3~4 MCU clock cycles until system clock ON and work. 0: MCU clock is On.
1	SOURCE_CLK_OFF (bias OFF)	1: SOURCE clock is Off. SOURCE clock sources: (MCU clock is closed and bias OFF) (1) External 12/24 MHz or 32.768 kHz crystal oscillator, and MCU must wait for 16385~16386 SYSTEM clock cycles until source clock ON and work. (2) Internal 12 MHz IRC oscillator, and MCU must wait for 129~130 SYSTEM clock cycles until source clock ON and work. (3) Internal 32 kHz IRC oscillator, and MCU must wait for 9~10 SYSTEM clock cycles until source clock ON and work. 0: MCU clock is On.
0	IRC 12M_CLK_OFF (bias ON)	1: Internal 12 MHz RC oscillator is Off and bias ON MCU must wait for 11~12 IRC12M clock+IRC start-up (about 10 s) cycles until source clock ON and work. 0: MCU clock is On.

-: unimplemented.

Note: Refer to section 3.1 System Clock Tree for more details.

Clock Source Control Register IRC_12M_PD (XFR: 0x07) **Reset Value: A3h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	R/W	R/W	R/W	R/W	R/W
Name	Reserved			IRC_12M_PD1	IRC_12M_PD2	IRC_32K_PD	CRY_12M_PD	CRY_32K_PD

Bit Number	Bit Mnemonic	Description
7-5	-	Must be equal to “101”, otherwise bit[4:0] cannot be written into
4	IRC_12M_PD1	1: partial internal 12 MHz RC oscillator power is turned off (bias ON) (default value is not off) 0: not off
3	IRC_12M_PD2	1: all internal 12 MHz RC oscillator power is turned off (bias off) (default value is not off) 0: not off
2	IRC_32K_PD	1: internal 32 kHz RC oscillator power is turned off (default value is not off)

Bit Number	Bit Mnemonic	Description
		0: not off
1	CRY_12M_PD	1: external 12 MHz crystal oscillator power is turned off (default value is off) 0: not off
0	CRY_32K_PD	1: external 32.768 kHz crystal oscillator power is turned off (default value if off) 0: not off

-: unimplemented.

Oscillator Driver Control Register CRY_12M_DR[1:0] (XFR: 0x08) **Reset Value: 54h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	R/W	R/W	R/W
Name	Reserved				Reserved	CRY_12M_DR[1:0]		BLDO_PD

Bit Number	Bit Mnemonic	Description
7-4	-	Must be equal to “0101”, otherwise, Bit[3:0] cannot be written into
3	Reserved	-
2-1	CRY_12M_DR[1:0]	External oscillator driving ability setting 00: crystal oscillator with frequency of 32768 Hz 01: crystal oscillator with frequency of 100 kHz ~ 1 MHz 10: crystal oscillator with frequency of 1 MHz ~ 12 MHz (default) 11: crystal oscillator with frequency of 12 MHz ~ 24 MHz Default value can be selected by section 6.19 Code Option Select
0	BLDO_PD	Internal voltage regulator (main LDO) 1: turn off main LDO 0: turn on main LDO (default) Default value can be selected by section 6.19 Code Option Select

-: unimplemented.

Note: Main LDO is turned off only on Green mode, if SOURCE clock is 12 MHz (IRC internal or external crystal oscillator) must be turned on, otherwise will result in failure and cannot program.

Path Selection Control Register PATH_SLT (XFR: 0x0B) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	-	-	R/W
Name	IRQ_SLT[3:0]				Reserved			BGP_VOL_SLT

Bit Number	Bit Mnemonic	Description
7-4	IRQ_SLT[3:0]	Select IRQ 0~3 path 1: set IRQx as Path B 0: set IRQx as Path A
3-1	Reserved	-
0	BGP_VOL_SLT	BANDGAP Voltage selection 1: BANDGAP = 2.44V 0: BANDGAP = 1.22V

-: unimplemented.

General-purpose I/O Port A Wakeup Control Register GPIOA_WK[7:0] (XFR: 0x60) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_WK[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOA_WK[7:0]	General-purpose I/O Port A Wakeup MCU Enable setting Bit 7 = 1: Enable General-purpose I/O Port A7 Wakeup MCU function; 0: function disabled Bit 6 = 1: Enable General-purpose I/O Port A6 Wakeup MCU function; 0: function disabled Bit 5 = 1: Enable General-purpose I/O Port A5 Wakeup MCU function; 0: function disabled Bit 4 = 1: Enable General-purpose I/O Port A4 Wakeup MCU function; 0: function disabled Bit 3 = 1: Enable General-purpose I/O Port A3 Wakeup MCU function; 0: function disabled Bit 2 = 1: Enable General-purpose I/O Port A2 Wakeup MCU function; 0: function disabled Bit 1 = 1: Enable General-purpose I/O Port A1 Wakeup MCU function; 0: function disabled Bit 0 = 1: Enable General-purpose I/O Port A0 Wakeup MCU function; 0: function disabled

General-purpose I/O Port B Wakeup Control Register GPIOB_WK[7:0] (XFR: 0x61) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_WK[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOB_WK[7:0]	General-purpose I/O Port B Trigger Wakeup MCU Enable setting Bit 7 = 1: Enable General-purpose I/O Port B7 Trigger Wakeup MCU function; 0: function disabled Bit 6 = 1: Enable General-purpose I/O Port B6 Trigger Wakeup MCU function; 0: function disabled Bit 5 = 1: Enable General-purpose I/O Port B5 Trigger Wakeup MCU function; 0: function disabled Bit 4 = 1: Enable General-purpose I/O Port B4 Trigger Wakeup MCU function; 0: function disabled Bit 3 = 1: Enable General-purpose I/O Port B3 Trigger Wakeup MCU function; 0: function disabled Bit 2 = 1: Enable General-purpose I/O Port B2 Trigger Wakeup MCU function;

Bit Number	Bit Mnemonic	Description
		0: function disabled Bit 1 = 1: Enable General-purpose I/O Port B1 Trigger Wakeup MCU function; 0: function disabled Bit 0 = 1: Enable General-purpose I/O Port B0 Trigger Wakeup MCU function; 0: function disabled

General-purpose I/O Port E Wakeup Control Register GPIOE_WK[7:0] (XFR: 0x62) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOE_WK[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOE_WK[7:0]	General-purpose I/O Port E Trigger Wakeup MCU Enable setting Bit 7 = 1: Enable General-purpose I/O Port E7 Trigger Wakeup MCU function; 0: function disabled Bit 6 = 1: Enable General-purpose I/O Port E6 Trigger Wakeup MCU function; 0: function disabled Bit 5 = 1: Enable General-purpose I/O Port E5 Trigger Wakeup MCU function; 0: function disabled Bit 4 = 1: Enable General-purpose I/O Port E4 Trigger Wakeup MCU function; 0: function disabled Bit 3 = 1: Enable General-purpose I/O Port E3 Trigger Wakeup MCU function; 0: function disabled Bit 2 = 1: Enable General-purpose I/O Port E2 Trigger Wakeup MCU function; 0: function disabled Bit 1 = 1: Enable General-purpose I/O Port E1 Trigger Wakeup MCU function; 0: function disabled Bit 0 = 1: Enable General-purpose I/O Port E0 Trigger Wakeup MCU function; 0: function disabled

General-purpose I/O Port F Wakeup Control Register GPIOF_WK[3:0] (XFR: 0x63) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOF_WK[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOF_WK[7:0]	General-purpose I/O Port F Trigger Wakeup MCU Enable setting Bit 7 = 1: Enable General-purpose I/O Port F7 Trigger Wakeup MCU function;

Bit Number	Bit Mnemonic	Description
		0: function disabled Bit 6 = 1: Enable General-purpose I/O Port F6 Trigger Wakeup MCU function; 0: function disabled Bit 5 = 1: Enable General-purpose I/O Port F5 Trigger Wakeup MCU function; 0: function disabled Bit 4 = 1: Enable General-purpose I/O Port F4 Trigger Wakeup MCU function; 0: function disabled Bit 3 = 1: Enable General-purpose I/O Port F3 Trigger Wakeup MCU function; 0: function disabled Bit 2 = 1: Enable General-purpose I/O Port F2 Trigger Wakeup MCU function; 0: function disabled Bit 1 = 1: Enable General-purpose I/O Port F1 Trigger Wakeup MCU function; 0: function disabled Bit 0 = 1: Enable General-purpose I/O Port F0 Trigger Wakeup MCU function; 0: function disabled

-: unimplemented.

Peripheral Interrupt Wakeup Control Register PERIPHERAL_WK (XFR: 0x64) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
Name	INT_WK[3:0]				ADC_WK	ACOMP_WK	WTMR_WK	Reserved

Bit Number	Bit Mnemonic	Description
7-4	INT_WK[3:0]	External 8052 INT0/1/2/3 Wakeup MCU Enable setting Bit 7 = 1: Enable 8052 INT3 Wakeup MCU function; 0: function disabled Bit 6 = 1: Enable 8052 INT2 Wakeup MCU function; 0: function disabled Bit 5 = 1: Enable 8052 INT1 Wakeup MCU function; 0: function disabled Bit 4 = 1: Enable 8052 INT0 Wakeup MCU function; 0: function disabled
3	ADC_WK	ADC compare mode Wakeup MCU Enable setting 1: Enable Wakeup MCU function after ADC compare is complete 0: Disable Wakeup MCU function after ADC compare is complete
2	ACOMP_WK	Comparator Wakeup MCU Enable setting 1: Enable Wakeup MCU function after Comparator is triggered 0: Disable Wakeup MCU function after Comparator is triggered
1	WTMR_WK	Watch Timer Wakeup MCU Enable setting 1: Enable Watch Timer Wakeup MCU function after Watch Timer is triggered 0: Disable Watch Timer Wakeup MCU function after Watch Timer is triggered
0	Reserved	-

-: unimplemented.

General-purpose I/O Port A Wakeup Flag Register GPIOA_TOG[7:0] (XFR: 0x65) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	GPIOA_TOG[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOA_TOG[7:0]	General-purpose I/O Port A Trigger Wakeup Flag. If the corresponding bit Toggle Trigger occurred, Wakeup Flag Bit = 1 Bit 7: I/O Port A7 Wakeup Flag Bit 6: I/O Port A6 Wakeup Flag Bit 5: I/O Port A5 Wakeup Flag Bit 4: I/O Port A4 Wakeup Flag Bit 3: I/O Port A3 Wakeup Flag Bit 2: I/O Port A2 Wakeup Flag Bit 1: I/O Port A1 Wakeup Flag Bit 0: I/O Port A0 Wakeup Flag

General-purpose I/O Port B Wakeup Flag Register GPIOB_TOG[7:0] (XFR: 0x66) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	GPIOB_TOG[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOB_TOG[7:0]	General-purpose I/O Port B Trigger Wakeup Flag. If the corresponding bit Toggle Trigger occurred, Wakeup Flag Bit = 1 Bit 7: I/O Port B7 Wakeup Flag Bit 6: I/O Port B6 Wakeup Flag Bit 5: I/O Port B5 Wakeup Flag Bit 4: I/O Port B4 Wakeup Flag Bit 3: I/O Port B3 Wakeup Flag Bit 2: I/O Port B2 Wakeup Flag Bit 1: I/O Port B1 Wakeup Flag Bit 0: I/O Port B0 Wakeup Flag

General-purpose I/O Port E Wakeup Flag Register GPIOE_TOG[7:0] (XFR: 0x67) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	GPIOE_TOG[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOE_TOG[7:0]	General-purpose I/O Port E Trigger Wakeup Flag. If the corresponding bit Toggle Trigger occurred, Wakeup Flag Bit = 1 Bit 7: I/O Port E7 Wakeup Flag Bit 6: I/O Port E6 Wakeup Flag Bit 5: I/O Port E5 Wakeup Flag Bit 4: I/O Port E4 Wakeup Flag Bit 3: I/O Port E3 Wakeup Flag

Bit Number	Bit Mnemonic	Description
		Bit 2: I/O Port E2 Wakeup Flag Bit 1: I/O Port E1 Wakeup Flag Bit 0: I/O Port E0 Wakeup Flag

General-purpose I/O Port F Wakeup Flag Register GPIOF_TOG[3:0] (XFR: 0x68) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	GPIOF_TOG[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOF_TOG[7:0]	General-purpose I/O Port F Trigger Wakeup Flag. If the corresponding bit Toggle Trigger occurred, Wakeup Flag Bit = 1 Bit 7: I/O Port F7 Wakeup Flag Bit 6: I/O Port F6 Wakeup Flag Bit 5: I/O Port F5 Wakeup Flag Bit 4: I/O Port F4 Wakeup Flag Bit 3: I/O Port F3 Wakeup Flag Bit 2: I/O Port F2 Wakeup Flag Bit 1: I/O Port F1 Wakeup Flag Bit 0: I/O Port F0 Wakeup Flag

-: unimplemented.

Peripheral Interrupt Wakeup Flag Register PERIPHERAL_TOG (XFR: 0x69) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	-
Name	INT_WK_EVT[3:0]				ADC_TOG	ACOMP_TOG	WTMR_EVT	Reserved

Bit Number	Bit Mnemonic	Description
7-4	INT_WK_EVT[3:0]	Interrupt Wakeup Flag Bit 7 = 1: MCU is waken up by INT3 interrupt Bit 6 = 1: MCU is waken up by INT2 interrupt Bit 5 = 1: MCU is waken up by INT1 interrupt Bit 4 = 1: MCU is waken up by INT0 interrupt
3	ADC_TOG	ADC Compare mode Trigger (Wakeup) Flag 1: a Trigger (Wakeup) occurred in ADC compare mode 0: a Trigger (Wakeup) not occurred in ADC compare mode
2	ACOMP_TOG	Comparator Trigger (Wakeup) Flag 1: a Trigger (Wakeup) occurred in Comparator 0: a Trigger (Wakeup) not occurred in Comparator
1	WTMR_EVT	Watch Timer Trigger (Wakeup) Flag 1: a Trigger (Wakeup) occurred in Watch Timer 0: a Trigger (Wakeup) not occurred in Watch Timer
0	Reserved	-

-: unimplemented.

Wakeup Clear Register CLR_IN_TOG (XFR: 0x6A) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	-	-	-	-	-	-	R
Name	CLR_IN_TOG	Reserved						IN_TOG

Bit Number	Bit Mnemonic	Description
7	CLR_IN_TOG	1: Clear all Input Toggle
6-1	Reserved	-
0	IN_TOG	1: All toggle events logic- or operation if any toggle source occurred, this bit will be set.

-: unimplemented.

The setting of entering Sleep Mode and Wakeup procedure:

1. Set RST_NDF = 1
2. Disable Watchdog Timer (DIS_WDT[7:5] = 101)
3. Select Wakeup sources:

		Sleep Mode	Idle Mode	
Wakeup Sources		**No Clock**	**Sub: 32 kHz**	**Main: 12 MHz**
1.	NRST pin is low voltage	●	●	●
2.	External Interrupt INT0/1/2 sources			
	➢ SPI interrupt			●
	➢ Comparator interrupt			●
	➢ Low Voltage Detection interrupt	●	●	●
	➢ Watch Timer interrupt			
	➢ Enhanced Timer/Counter interrupt			●
	➢ **32** General-purpose I/O pin Toggle interrupt	●	●	●
3.	External interrupt INT3 sources (GPIO A/B/E/F)			
	➢ 16 IRQ interrupt pins			
4.	28 General-purpose I/O pin Toggle interrupt (GPIO A/B/E/F)	●	●	●
5.	ADC_WK (Compare Mode)	●	●	●
6.	ACOMP_WK	●	●	●
7.	WTMR_WK	●	●	●

4. Select internal 12 MHz RC oscillator as SOURCE clock (SOURCE_CLK_SLT[1:0] = 00)
   (4-A) Clear HFIRC_CLK_SLT (XFR_0x01 bit2)
   (4-B) Move Flash memory XDATA 0x0E03 to register XFR-0x70
5. Clear all input Trigger Wakeup (CLR_IN_TOG = 1)
6. Enter Sleep Mode (SOURCE_CLK_OFF = 1)
7. Wait for Wakeup Trigger

   SOURCE clock = IRC 12M, needs to wait for 128 clock cycles to return to the main program
   SOURCE clock = Crystal, needs to wait for 16 x 1024 clock cycles to return to the main program
   (7-A) Set HFIRC_CLK_SLT (XFR_0x01 bit2)
   (7-B) Move Flash memory XDATA 0x0E07 to register XFR-0x70

   * (4-A), (4-B), (7-A), and (7-B) need to be executed only in IRC 24M.
   * If Source Clock = IRC oscillator, please switch to IRC 12 MHz to ensure wakeup function before entering Sleep1/Sleep2 mode.

6.8 12/24 MHz RC Oscillator Calibration

WT56F248/232 has a built-in 12/24 MHz RC oscillator to reduce the cost of external crystal oscillator. For more precise system clock, external crystal oscillator 12/24 MHz is available. In addition, it is a better choice to use 32.768 kHz (crystal oscillator) to calibrate internal RC 12/24 MHz oscillators. (Calibration can reach ±1% at -40℃ ~ +105℃)

Internal Oscillator Adjust Register RC_LADJ (XFR: 0x70) **Reset Value: 40h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	RC_LADJ_C[2:0]			RC_LADJ_F[3:0]			

Bit Number	Bit Mnemonic	Description
7	Reserved	-
6-4	RC_LADJ_C[2:0]	Each level 8% coarse adjustment of the Internal RC oscillator frequency (default value '100'), 7 levels in total
3-0	RC_LADJ_F[3:0]	Each level 0.5% fine adjustment of the Internal RC oscillator frequency (default value '1000'), 15 levels in total

-: unimplemented.

Note: Internal Oscillator Adjustment Register RC_LADJ_C[2:0] & RC_LADJ_F[3:0] is allowed to adjust the control circuit of IRC 12 MHz directly.

Internal Oscillator Counter Data High Bytes Register RC12M_CNT[9:2] (XFR: 0x71) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	RC12M_CNT[9:2]							

Bit Number	Bit Mnemonic	Description
7-0	RC12M_CNT[9:2]	The counting value RC12M_CNT[9:2] of internal 12/24 MHz RC oscillator, is paired with RC12M_CNT[1:0] to form a 10-bit counting value

Internal Oscillator Counter Data Low Bytes Register RC12M_CNT[1:0] (XFR: 0x72) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R	R
Name	Reserved						RC12M_CNT[1:0]	

Bit Number	Bit Mnemonic	Description
7-2	Reserved	-
1-0	RC12M_CNT[1:0]	The counting value RC12M_CNT[1:0] of internal 12/24 MHz RC oscillator, is paired with RC12M_CNT[9:2] to form a 10-bit counting value

-: unimplemented.

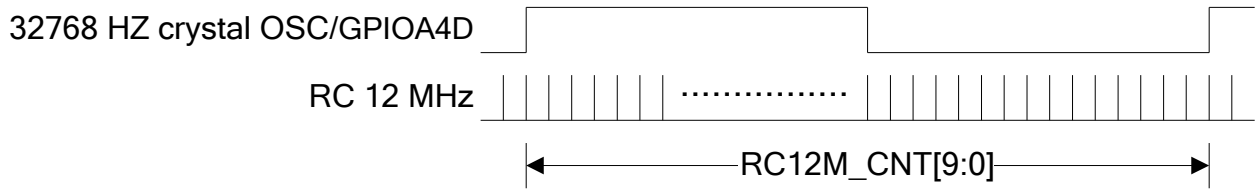
Internal Oscillator Calibration Control Register RC_CALIB_EN (XFR: 0x73) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	-	R/W	-	-	-	-	-
Name	RC_CALIB_EN	Reserved	AUTO_CAL_EN	Reserved				

Bit Number	Bit Mnemonic	Description
7	RC_CALIB_EN	1: Enable RC Oscillator Calibration function
6	Reserved	-
5	AUTO_CAL_EN	1: Enable H/W automatic calibration function
4-0	Reserved	-

-: unimplemented.

Note:
Manual calibration: enable RC_CALIB_EN, and is working together with Firmware.
Automatic calibration: enable RC_CALIB_EN and AUTO_CAL_EN.



Calibration Theory:

When the external 32.768 kHz oscillator is used, it is available to count in the fixed width of precise 32.768 kHz by internal RC 12/24 MHz. Then with the counting value we got, we can make a compensation by controlling the Internal Oscillator Adjust Registers RC_LADJ_C [2:0] & RC_LADJ_F [3:0], reaching ±1% at room temperature.

The range of coarse adjustment and fine adjustment:

Coarse adjustment: the actual internal RC frequency ± (internal RC frequency * 0.08); RC_LADJ_C[2:0] ranges from 000 ~ 111, and the middle value is 100.

Fine adjustment: the actual internal RC frequency ± (internal RC frequency * 0.005); RC_LADJ_F[3:0] ranges from 0000 ~ 1111, and the middle value is 1000.

RC 12MHz

RC12M_CNT[9:0]	External 32.768 kHz Sampled (Hz)	Target Value (Hz)	Tolerance %
360	11796480	12000000	+1.70
361	11829248	12000000	+1.42
362	11862016	12000000	+1.15
363	11894784	12000000	+0.88
364	11927552	12000000	+0.60
365	11960320	12000000	+0.33

RC12M_CNT[9:0]	External 32.768 kHz Sampled (Hz)	Target Value (Hz)	Tolerance %
366	11993088	12000000	+0.06
367	12025856	12000000	-0.22
368	12058624	12000000	-0.49
369	12091392	12000000	-0.76
370	12124160	12000000	-1.03

RC 24MHz

RC12M_CNT[9:0]	External 32.768 kHz Sampled (Hz)	Target Value (Hz)	Tolerance %
727	23822336	24000000	-0.74
728	23855104	24000000	-0.6
729	23887872	24000000	-0.47
730	23920640	24000000	-0.33
731	23953408	24000000	-0.19
732	23986176	24000000	-0.06
733	24018944	24000000	0.08
734	24051712	24000000	0.22
735	24084480	24000000	0.35
736	24117248	24000000	0.49
737	24150016	24000000	0.63

Notes:

1. When WT56F248/232 is waken up from sleep mode (RC bias is turned on), RC oscillator calibration function needs to wait for at least 83.3ns (at 12 MHz) to return to normal mode.
2. As soon as the RC oscillator calibration function is enabled, read RC12M_CNT[9:2] & RC12M_CNT[1:0] registers twice, then confirm the data is the same to proceed with the calibration process.
3. If RC12M_CNT[9:0] internal oscillator counter data register is 511 (0x1FF), indicating that no external oscillator or without enabling external oscillator.
4. When reset, WT56F248/232 will auto-reload the calibration value of RC 12 MHz into internal oscillator adjustment register (XFR: 0x70).

   To switch to RC 24 MHz, HFIRC_CLK_SLT (XFR_0x01_bit2) must be set by program and load the corresponding calibration value.

   IRC Oscillator (12/24M) switching procedures:

   (a) IRC12M change to IRC24M
   - (1) Set HFIRC_CLK_SLT
   - (2) Move flash memory XDATA 0x0E07H-bit[6:0] to XFR_0x70 register

   (b) IRC24M change to IRC12M
   - (1) Clear HFIRC_CLK_SLT
   - (2) Move flash memory XDATA 0x0E03H-bit[6:0] to XFR_0x70 register

5. When enable AUTO_CAL_EN & the external 32.768 kHz oscillator of MCU is also oscillated, MCU will also calibrate once every 30.5us.
   (condition: CRY_32K_PD, IRC_12M_PD1 & IRC_12M_PD2 cannot be turned off)

6.9 Watchdog Timer and Watch Timer

6.9.1 Watchdog Timer (WDT)

Watchdog Timer can be used to detect CPU failures, such as the software deadlock circles caused by noises, voltage disturbance, or power off etc. When an internal counter of the Watchdog Timer overflows, a reset signal will be generated then reset the CPU.

Watchdog Timer is not similar to the general-purpose 8052 Timer 0/1/2. To prevent a reset occurred on Watchdog Timer, which can be cleared by software before important path of program. When unpredictable reset occurred, user should check the WDT_RST_FLG bit in Reset Flag Register to judge if the previous reset is occurred by Watchdog Timer.

- Clock sources of Watchdog Timer: Internal 32 kHz, or External 32.768 kHz Crystal Oscillator
- Reset Time: 16 ms, 32 ms, 1.024 S or 2.048 S

Watchdog Timer Control Register WDT_CTL (XFR: 0x78) **Reset Value: 02h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	-	-	-	R/W	R/W
Name	DIS_WDT[2:0]			Reserved			WDT_TM_SLT[1:0]	

Bit Number	Bit Mnemonic	Description
7-5	DIS_WDT[2:0]	Watchdog Timer switch 101: Disable Watchdog Timer at the same time clear counts Other value: Enable Watchdog Timer
4-2	Reserved	-
1-0	WDT_TM_SLT[1:0]	Watchdog Reset Time setting When the Watchdog uses internal RC 32 kHz oscillator: 00: 16 ms 01: 32 ms 10: 1.024 S 11: 2.048 S When the Watchdog uses external 32.768 kHz Crystal Oscillator: 00: 15.625 ms 01: 31.25 ms 10: 1 S 11: 2 S

-: unimplemented.

Notes:

1. The frequency tolerance of internal 32 kHz RC oscillator is about ±30%.
2. The Watchdog Timer clock sources can be selected by the bit WDT_CLK_SLT of System Control Register (XFR: 0x01), with details as below.

System Control Register SYS_CTL (XFR: 0x01) **Reset Value: 90h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	-	R/W		R/W	R/W	R/W
Name	RST_NDF	LVR_PD	Reserved	SPEEDUP_C32K[1:0]		HFIRC_CLK_SLT	WDT_CLK_SLT	WTMR_CLK_SLT

Bit Number	Bit Mnemonic	Description
7	RST_NDF	1: NRST pin without digital filter function in 0: NRST pin with digital filter function (4 clocks)
6	LVR_PD	1: turn off low voltage reset power 0: turn on low voltage reset power
5	Reserved	This bit must be set as 0.
4-3	SPEEDUP_C32K[1:0]	Speed up 32.768 kHz crystal oscillator 10: the second-biggest current (default) Others: reserved
2	HFIRC_CLK_SLT	1: set IRC oscillator = 24 MHz 0: set IRC oscillator = 12 MHz
1	WDT_CLK_SLT	1: Watchdog Timer uses external 32.768 kHz crystal oscillator 0: Watchdog Timer uses internal 32 kHz RC oscillator
0	WTMR_CLK_SLT	1: Watch Timer uses external 32.768 kHz crystal oscillator 0: Watch Timer uses internal 32 kHz RC oscillator

-: unimplemented.

6.9.2 Watch Timer

The application functions of Watch Timer include Timer Interrupt, Timer Wakeup, Timer ADC, Buzzer Output, LCD display frequency and so on.

- The clock source of Watch Timer is 32 kHz internal RC oscillator or 32.768 kHz external oscillator. By this clock, it can generate 8 Time base
- Watch Timer can also generate a stable 0.5 kHz, 1 kHz, 2 kHz or 4 kHz frequency signal for Buzzer to produce sound
- Watch Timer can also be served as the display frequency sources of LCD Driver, with 5 frequencies to select. (Refer to LCD Driver section)

Watch Timer Control Register WTMR_CTL (XFR: 0x7C) **Reset Value: 80h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R	W	-	-	-	-	-
Name	DIS_WTMR	WTMR_EVT	CLR_WTMR_EVT	Reserved				

Bit Number	Bit Mnemonic	Description
7	DIS_WTMR	1: disable Watch Timer 0: enable Watch Timer
6	WTMR_EVT	1: indicates Watch Timer Event (the setting time of Watch Timer as the count reaches WTMER[2:0]) 0: cleared by CLR_WTMR_EVT = 1

Bit Number	Bit Mnemonic	Description
5	CLR_WTMR_EVT	1: Clear Watch Timer event, and then WTMR_EVT = 0
4-0	Reserved	-

-: unimplemented.

Watch Timer Output Selection Register WTMR_SLT[2:0] (XFR: 0x7D) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	R/W	R/W	-	R/W	R/W	R/W
Name	Reserved		BUZER_SLT[1:0]		Reserved	WTMR_SLT[2:0]		

Bit Number	Bit Mnemonic	Description
7-6	Reserved	-
5-4	BUZER_SLT[1:0]	Buzzer signal selection bit (IRC 32 kHz or Crystal Oscillator 32.768 kHz) 00: 0.5 kHz 01: 1 kHz 10: 2 kHz 11: 4 kHz
3	Reserved	-
2-0	WTMR_SLT[2:0]	Watch Timer Time base selection bit (If needs to be precise, using external Crystal Oscillator 32.768 kHz) is recommended. 000: watch time = 3.91 ms 001: watch time = 31.25 ms 010: watch time = 62.50 ms 011: watch time = 125 ms 100: watch time = 0.25 S 101: watch time = 0.5 S 110: watch time = 1 S 111: watch time = 2 S

-: unimplemented.

The Buzzer signal output of WT56F248/232 is determined by Register. Select 3 paths (BUZOA, BUZOB or BUZOC) for output.

Buzzer	Register Setting	Output pin
BUZOA	(XFR: 0x2F) GPF0_FUN_SLT[1:0] = 11	GPIOF0
BUZOB	(XFR: 0x27) GPB6_FUN_SLT[1:0] = 01	GPIOB6
BUZOC	(XFR: 0x2E) GPE3_FUN_SLT[1:0] = 10	GPIOE3

The related switch controls are described below:

1. Enable Buzzer Output: Control Complex Function Register. Switch general-purpose I/O port as Buzzer pin, and then WT56F248/232 will output the frequency based on the setting of BUZER_SLT[1:0].
2. Disable Buzzer Output: Control Complex Function Register. Switch Buzzer pin to general-purpose I/O port or turn off Watch Timer (DIS_WTMR), the output stops.

6.10 LCD Driver

WT56F248/232 contains LCD driver and control Circuit to drive LCD panel directly. Internal RC 32 kHz or external 32.768 kHz oscillator is available for LCD system clock source selection, and Watch Timer must be enabled.

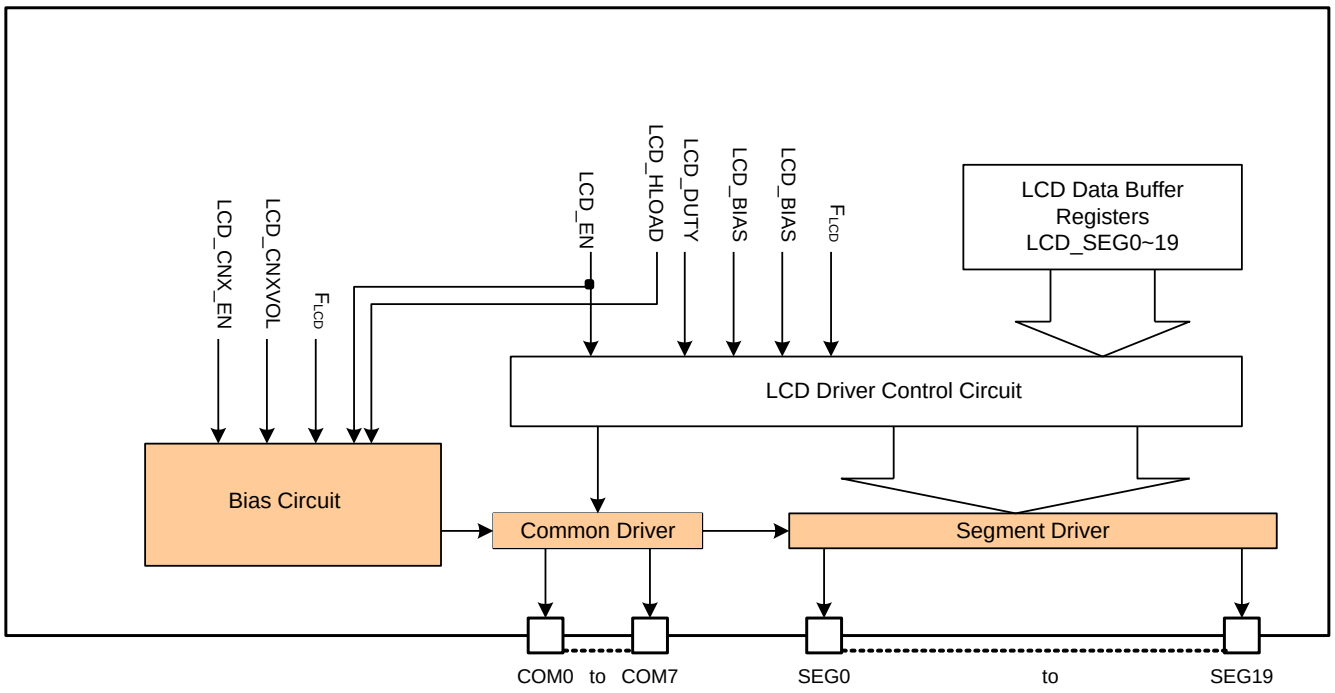
WT56F248/232 supports two types of LCD driver:

Mode A: 8 x 19 dots with below features:

- Built-in LCD Bias Voltages circuit with three selectable bias: 1/3, or 1/4 Bias
- Internal Register supports Duty Cycles adjustment: 1/3, 1/4, or 1/8 Duty
- Internal Register supports 30 levels of Contrast Adjustment
- Duty cycle/Bias/Frequency can be set by software

Mode B: 4 x 20 dots or 8 x 16 dots with below features:

- Built-in LCD Bias Voltages circuit with three selectable bias: 1/3, or 1/4 Bias
- Internal Register supports Duty Cycles adjustment: 1/3, 1/4, or 1/8 Duty
- Internal Register supports 30 levels of Contrast Adjustment
- Duty cycle/Bias/Frequency can be set by software
- The display frequency source of LCD Driver is Watch Timer, please refer to 6.9.2 Watch Timer



LCD Driver Control Register 1 LCD_CTL1 (XFR: 0x98) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	-	-	-
Name	LCD_EN	LCD_HLOAD	LCD_SEL	LCD_VBUF_EN	Reserved			

Bit Number	Bit Mnemonic	Description
7	LCD_EN	LCD Power Control (During setting the related register of the LCD Driver, turning off the LCD power is essential.) 1: turn on LCD Driver power 0: turn off LCD Driver power
6	LCD_HLOAD	LCD Driver Load selection 1: heavy load (internal resistor sum up: 120KΩ) 0: normal load (internal resistor sum up: 480KΩ)
5	LCD_SEL	LCD Driver output pin selection 1: LCD Driver Mode B output (BSEG0~19, BCOM0~7) (can replace ABOV MC80F7708) 0: LCD Driver Mode A output (ASEG0~18, ACOM0~7) (can replace Samsung S3F9488)
4	LCD_VBUF_EN	LCD driver buffer control 1: LVCD buffer out 0: LVCD normal out
3-0	Reserved	-

-: unimplemented.

Note: If LCD Driver selects Mode B output, I/O port Complex function selects Mode A output (ASEG0-18, ACOM0-7), then I/O is Output Tri-State; If LCD Driver selects Mode A output, I/O port Complex function selects Mode B output (BSEG0-19, BCOM0-7), then I/O is Output Tri-State.

LCD Driver Control Register 2 LCD_CTL2 (XFR: 0x99) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	LCD_CLK[2:0]			LCD_BIAS[1:0]		LCD_DUTY[1:0]	

Bit Number	Bit Mnemonic	Description
7	Reserved	-
6-4	LCD_CLK[2:0]	LCD Scanned Frequency setting. If external 32.768 kHz oscillator is selected as LCD system clock source, scanned frequency is 2048 Hz when set LCD_CLK[2:0] = 000 (please refer to “LCD Driver Frame frequency setting table” for more details). 000 = $fs/2^4$ (if fs = 32.768 kHz, lcd_clk = 2048 Hz) 001 = $fs/2^5$ 010 = $fs/2^6$ 011 = $fs/2^7$ 1xx = $fs/2^8$
3-2	LCD_BIAS[1:0]	LCD bias selection 00: 1/2 01: 1/3 10: 1/4 11: 1/5

Bit Number	Bit Mnemonic	Description
1-0	LCD_DUTY[1:0]	LCD duty selection 00: static 01: 1/3 duty 10: 1/4 duty 11: 1/8 duty

-: unimplemented.

LCD Driver Contrast Control Register LCD_CNXVOL[4:0] (XFR: 0x9A) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	R/W	R/W	R/W	R/W	R/W
Name	Reserved			LCD_CNXVOL[4:0]				

Bit Number	Bit Mnemonic	Description
7-5	Reserved	-
4-0	LCD_CNXVOL[4:0]	LCD Driver Contrast Voltage VLCD, with 30 levels for selection. 00000: VLCD = 1/2 VDD 00001: VLCD = VDD *(30/59) 00010: VLCD = VDD *(30/58) | 11101: VLCD = VDD *(30/31) 11110: VLCD = VDD *(30/30) 11111: VLCD = VDD $V_{LCD} = VDD \times \frac{30}{(60 - LCD\_CNXVOL[4:0])}$

-: unimplemented.

If V_{DD} = 5.0V, VLCD contrast voltage is as below:

LCD_CNXVOL[4:0]	VLCD	
00000	1/2 VDD	2.5V
00101	VDD*(30/55)	2.73V
01010	VDD*(30/50)	3.00V
01111	VDD*(30/50)	3.33V
10100	VDD*(30/40)	3.75V
11001	VDD*(30/35)	4.29V
11110	VDD*(30/30)	5.00V

LCD Driver Power-saving Control Register LCD_PSV_CTL (XFR: 0x9B) **Reset Value: 08h**

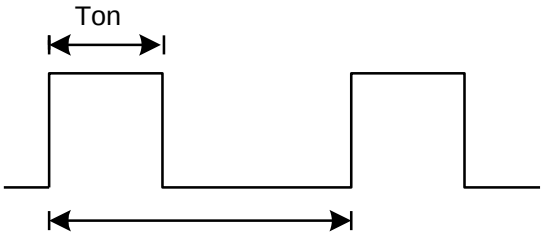
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	LCD_PSV_CTL	Reserved	LCD_PSVCK		LCD_PSDUTY			

Bit Number	Bit Mnemonic	Description
7	LCD_PSV_CTL	1: LCD Driver Power-saving mode 0: LCD Driver normal mode
6	Reserved	-
5-4	LCD_PSVCK[1:0]	Power Saving clock select 00: fs/2 01: $fs/2^2$ 10: $fs/2^3$ 11: $fs/2^4$
3-0	LCD_PSDUTY[3:0]	Power saving duty select Duty ratio = (LCD_PSDUTY setting)/16 x 100% LCD_PSDUTY[3:0] (The duty of voltage of LCD bias resistors) = 0001, Duty ratio = 6.25% = 1000, Duty ratio = 50% (default) = 1111, Duty ratio = 93.75%

-: unimplemented.

LCD bias resistors Voltage power-on time:

Ton = 1/ LCD_PSVCK x (LCD_PSDUTY)



LCD Driver Segment Output Enable Register 1 LCD_SEG_EN[7:0] (XFR: 0x9C) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	LCD_SEG_EN[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	LCD_SEG_EN[7:0]	SEGDx output enable setting; 1: SEGDx output 0000_0001: enable SEGD0 data output 0000_0011: enable SEGD1~0 data output | 0111_1111: enable SEGD6~0 data output 1111_1111: enable SEGD7~0 data output

LCD Driver Segment Output Enable Register 2 LCD_SEG_EN[15:8] (XFR: 0x9D) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	LCD_SEG_EN[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	LCD_SEG_EN[15:8]	SEGDx output enable setting; 1: SEGDx output 0000_0001: enable SEGD8 data output 0000_0011: enable SEGD9~8 data output | 0111_1111: enable SEGD14~8 data output 1111_1111: enable SEGD15~8 data output

LCD Driver Segment Enable Register 3 LCD_SEG_EN[19:16] (XFR: 0x9E) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				LCD_SEG_EN[19:16]			

Bit Number	Bit Mnemonic	Description
7-4	Reserved	-
3-0	LCD_SEG_EN[19:16]	SEGDx output enable setting; 1: SEGDx output 0001: enable SEGD16 data output 0011: enable SEGD17~16 data output 0111: enable SEGD18~16 data output 1111: enable SEGD19~16 data output

-: unimplemented.

Note: If the GPIO shared with SEG did not use SEG, the LCD SEG is allowed to set the output pin as output Tri-state by the enable Register LCD_SEG_EN[19:0].

LCD Driver Display Data Register 0~19 LCD_SEGDx[7:0] (XFR: 0x80 ~ 0x93) Reset Value: 00h
The table below is LCD display data Register mapping table:

4 COM LCD (COM0~3, SEG0~19)

Address	Register Name	7	6	5	4	3	2	1	0
						COM3	COM2	COM1	COM0
$80H	LCD_SEGD0[7:0]					SEG0	SEG0	SEG0	SEG0
$81H	LCD_SEGD1[7:0]					SEG1	SEG1	SEG1	SEG1
$82H	LCD_SEGD2[7:0]					SEG2	SEG2	SEG2	SEG2
$83H	LCD_SEGD3[7:0]					SEG3	SEG3	SEG3	SEG3
$84H	LCD_SEGD4[7:0]					SEG4	SEG4	SEG4	SEG4
$85H	LCD_SEGD5[7:0]					SEG5	SEG5	SEG5	SEG5
$86H	LCD_SEGD6[7:0]					SEG6	SEG6	SEG6	SEG6
$87H	LCD_SEGD7[7:0]					SEG7	SEG7	SEG7	SEG7
$88H	LCD_SEGD8[7:0]					SEG8	SEG8	SEG8	SEG8
$89H	LCD_SEGD9[7:0]					SEG9	SEG9	SEG9	SEG9
$8AH	LCD_SEGD10[7:0]					SEG10	SEG10	SEG10	SEG10
$8BH	LCD_SEGD11[7:0]					SEG11	SEG11	SEG11	SEG11
$8CH	LCD_SEGD12[7:0]					SEG12	SEG12	SEG12	SEG12
$8DH	LCD_SEGD13[7:0]					SEG13	SEG13	SEG13	SEG13
$8EH	LCD_SEGD14[7:0]					SEG14	SEG14	SEG14	SEG14
$8FH	LCD_SEGD15[7:0]					SEG15	SEG15	SEG15	SEG15
$90H	LCD_SEGD16[7:0]					SEG16	SEG16	SEG16	SEG16
$91H	LCD_SEGD17[7:0]					SEG17	SEG17	SEG17	SEG17
$92H	LCD_SEGD18[7:0]					SEG18	SEG18	SEG18	SEG18
$93H	LCD_SEGD19[7:0]					SEG19	SEG19	SEG19	SEG19

8 COM LCD (COM0~7, SEG0~19)

Address	Register Name	7	6	5	4	3	2	1	0
		COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
$80H	LCD_SEGD0[7:0]	SEG0	SEG0	SEG0	SEG0	SEG0	SEG0	SEG0	SEG0
$81H	LCD_SEGD1[7:0]	SEG1	SEG1	SEG1	SEG1	SEG1	SEG1	SEG1	SEG1
$82H	LCD_SEGD2[7:0]	SEG2	SEG2	SEG2	SEG2	SEG2	SEG2	SEG2	SEG2
$83H	LCD_SEGD3[7:0]	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3
$84H	LCD_SEGD4[7:0]	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4
$85H	LCD_SEGD5[7:0]	SEG5	SEG5	SEG5	SEG5	SEG5	SEG5	SEG5	SEG5
$86H	LCD_SEGD6[7:0]	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6
$87H	LCD_SEGD7[7:0]	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7
$88H	LCD_SEGD8[7:0]	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8
$89H	LCD_SEGD9[7:0]	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9
$8AH	LCD_SEGD10[7:0]	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10
$8BH	LCD_SEGD11[7:0]	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11
$8CH	LCD_SEGD12[7:0]	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12
$8DH	LCD_SEGD13[7:0]	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13
$8EH	LCD_SEGD14[7:0]	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14
$8FH	LCD_SEGD15[7:0]	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15
$90H	LCD_SEGD16[7:0]	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16
$91H	LCD_SEGD17[7:0]	SEG17	SEG17	SEG17	SEG17	SEG17	SEG17	SEG17	SEG17
$92H	LCD_SEGD18[7:0]	SEG18	SEG18	SEG18	SEG18	SEG18	SEG18	SEG18	SEG18
$93H	LCD_SEGD19[7:0]	SEG19	SEG19	SEG19	SEG19	SEG19	SEG19	SEG19	SEG19

LCD Duty Cycle & COM/SEG pin reference table:

LCD_SEL = 0	Static	1/3 duty	1/4 duty	1/8 duty
SEG	ASEG[18:0]	ASEG[18:0]	ASEG[18:0]	ASEG[18:0]
COM	ACOM[0]	ACOM[2:0]	ACOM[3:0]	ACOM[7:0]
LCD_SEL = 1	**Static**	**1/3 duty**	**1/4 duty**	**1/8 duty**
SEG	BSEG[19:0]	BSEG[19:0]	BSEG[19:0]	BSEG[15:0]
COM	BCOM[0]	BCOM[2:0]	BCOM[3:0]	BCOM[7:0]

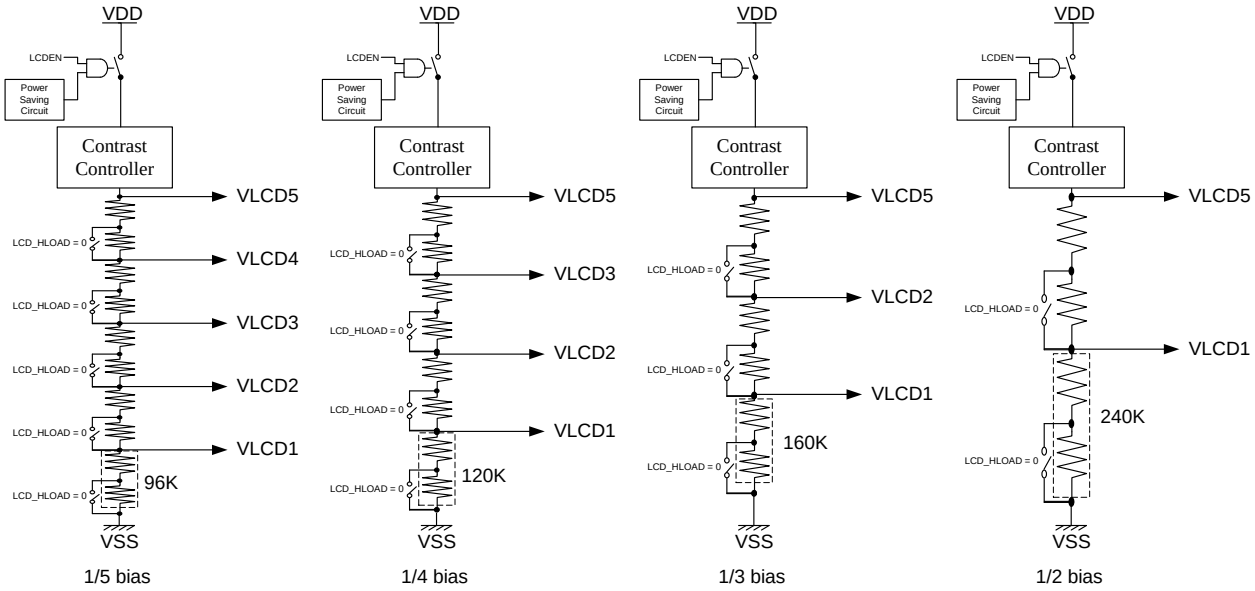
LCD Driver Bias table:

LCD Power Supply	Static	1/2	1/3	1/4	1/5
V_{LCD} = VLCD5	V_{LCD}	V_{LCD}	V_{LCD}	V_{LCD}	V_{LCD}
VLCD4	-	-	-	-	4/5 V_{LCD}
VLCD3	-	-	-	3/4 V_{LCD}	3/5 V_{LCD}
VLCD2	-	-	2/3 V_{LCD}	2/4 V_{LCD}	2/5 V_{LCD}
VLCD1	-	1/2 V_{LCD}	1/3 V_{LCD}	1/4 V_{LCD}	1/5 V_{LCD}
VSS	VSS	VSS	VSS	VSS	VSS

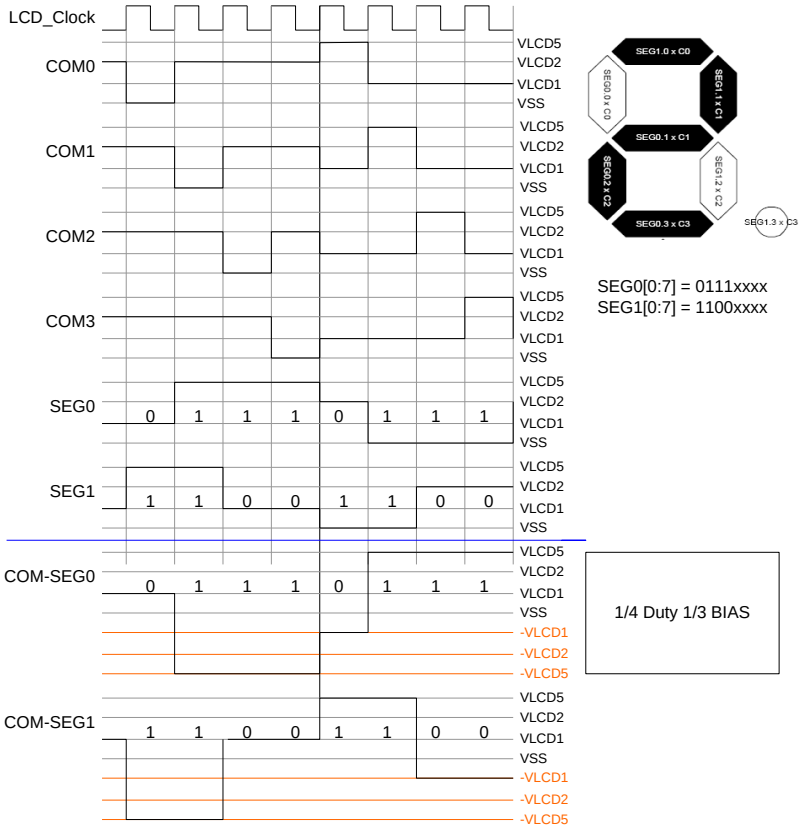
LCD Driver Frame frequency setting table:

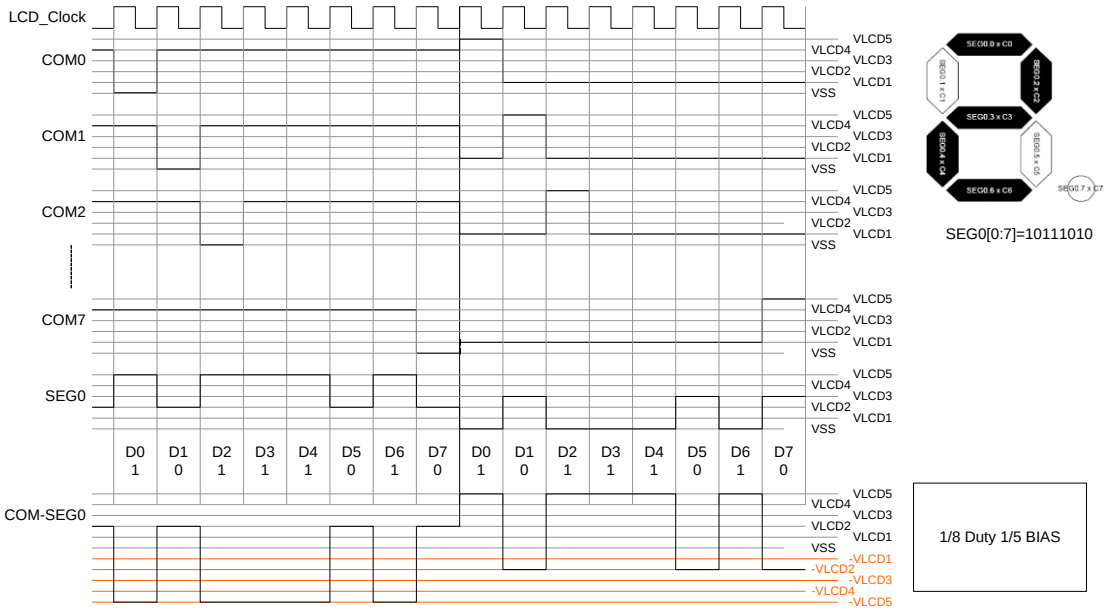
LCD_Frame (LCD_CLK[2:0])	LCD_CLK (Hz)	Frame Frequency (Hz)			
	Clock	Static	1/3 Duty	1/4 Duty	1/8 Duty
000	2048	1024	341	256	128
001	1024	512	171	128	64
010	512	256	85	64	32
011	256	128	43	32	16
1xx	128	64	21	16	8

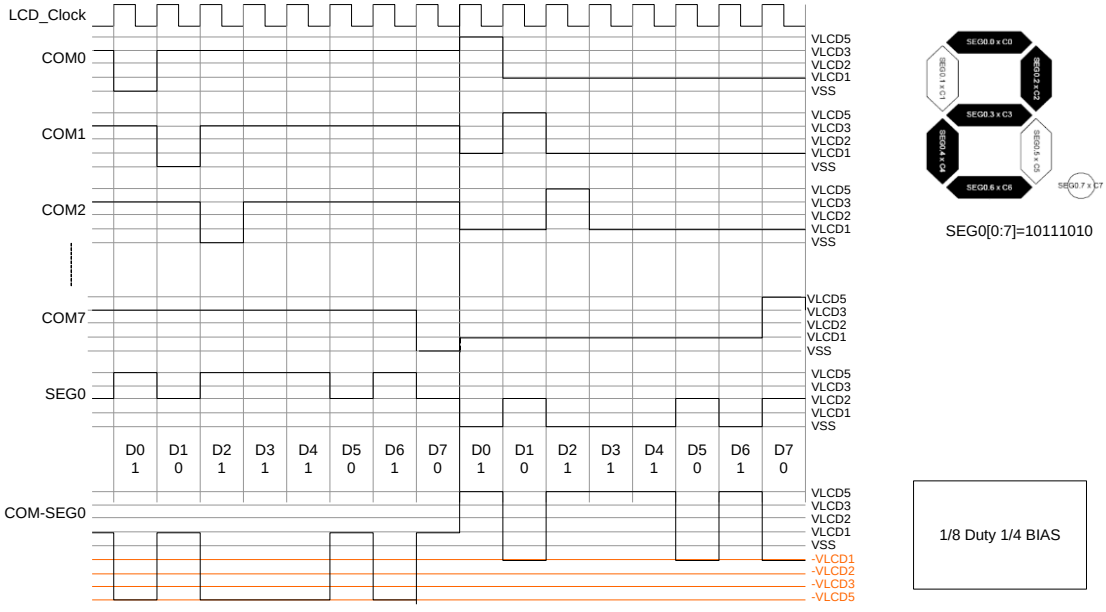
LCD bias voltage circuit with LCD_BIAS:



Note: LCD_HLOAD = 0 (sw: off): Normal Load; LCD_ HLOAD = 1 (sw: on): heavy Load







6.11 I²C Serial Interface

I²C module uses SCL (clock) and SDA (data) wires to connect with other I²C interfaces, the transmission is determined by the software programmed MI²C_CLK [1:0] in XFR, and is allowed to reach 400 KBps (maximum). I²C module also provide Master/Slave mode, and it is set by Register.

Master/Slave I²C Control Register MI²C_CTL (XFR: 0xA0) **Reset Value: 40h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	W	W	R/W	W	W
Name	MI²C_EN	MI²C_CLK[1:0]		MI²C_START	MI²C_STOP	MI²C_TXNAK	MI²C_CLR_RT	MI²C_CLR_STP

Bit Number	Bit Mnemonic	Description
7	MI²C _EN	1: enable I²C function 0: disable I²C function
6-5	MI²C _CLK[1:0]	Select Master I²C Clock 00: SCL clock = 400 kHz at 12 MHz oscillator 01: SCL clock = 200 kHz at 12 MHz oscillator 10: SCL clock = 100 kHz at 12 MHz oscillator 11: SCL clock = 50 kHz at 12 MHz oscillator
4	MI²C _START	1: enable I²C Transmit Start bit 0: disable I²C Transmit Start bit
3	MI²C _STOP	1: enable I²C Transmit Stop bit 0: disable I²C Transmit Stop bit
2	MI²C_TXNAK	Master I²C Transmit ACK bit after next Rx state 1: transmit NACK 0: transmit ACK
1	MI²C_CLR_RT	1: Clear Transmit and Receive interrupt
0	MI²C_CLR_STP	1: Clear Slave mode Stop status interrupt

Note: When changing the speed of master I²C, it requires 10us (SOURCE clock is 12 MHz) to stabilize the internal reference clock, and then the master I²C can go back to work.

Master/Slave I²C Status Register MI²C_STA (XFR: 0xA1) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	-
Name	MI²C_RDY	MI²C_INT_RT	MI²C_INT_STOP	MI²C_BB	MI²C_FIRST	MI²C_RW	MI²C_RXNAK	Reserved

Bit Number	Bit Mnemonic	Description
7	MI²C_RDY	When bit = 1, Interrupt status when I²C Receive/Transmit the 9th bit or Slave Stop phase
6	MI²C_INT_RT	When bit = 1, Interrupt status when I²C Receive/Transmit the 9th bit
5	MI²C_INT_STOP	When bit = 1, Interrupt status when I²C Slave mode Stop phase
4	MI²C_BB	When bit = 1, Slave mode bus busy

Bit Number	Bit Mnemonic	Description
3	MI²C_FIRST	Slave mode First phase. This is the first byte from Master I²C with specific Slave Address.
2	MI²C_RW	When bit = 1, Slave mode Read/Write Phase (the 8th bit of the first byte) 1: Slave I²C as Transmit mode 0: Slave I²C as Receive mode
1	MI²C_RXNAK	ACK bit indicator when I²C in Slave Tx mode 1: master mode return NACK (Slave will pull SAD high) 0: master mode return ACK
0	Reserved	-

-: unimplemented.

Master/Slave I²C Transmit Buffer Register MI²C_DSLV[7:0] (XFR: 0xA2) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MI²C_DSLV[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	MI²C_DSLV[7:0]	Master I²C transmit slave address buffer

Master/Slave I²C Transmit and Receive Buffer Register MI²C_DTRX[7:0] (XFR: 0xA3) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MI²C_DTRX[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	MI²C_DTRX[7:0]	I²C transmit and receive buffer W: When Tx work as I²C transmit buffer R: When Rx work as I²C receive buffer

Slave I²C Address Register MI²C_SADR (XFR: 0xA4) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MI²C_SADR							MI²C_SLVE

Bit Number	Bit Mnemonic	Description
7-1	MI²C_SADR	The slave address
0	MI²C_SLVE	I²C slave mode enable 1: I²C as Slave 0: I²C as Master

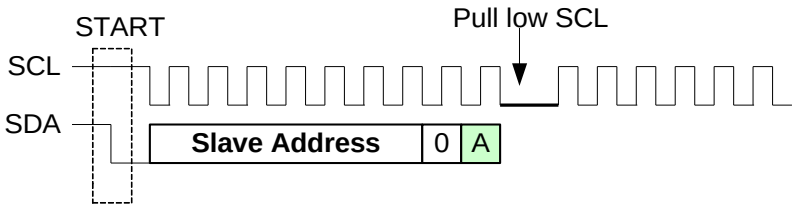
Master/Slave I²C Extended Control Register MI²C_EXTEND (XFR: 0xA5) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved						MI²C_AUTOSTP	MI²C_WAIT

Bit Number	Bit Mnemonic	Description
7-2	Reserved	-
1	MI²C_AUTOSTP	Enable Master I²C auto transmit stop bit, when receive NACK Bit
0	MI²C_WAIT	Enable Master/Slave I²C pull SCL low after the 9th bit

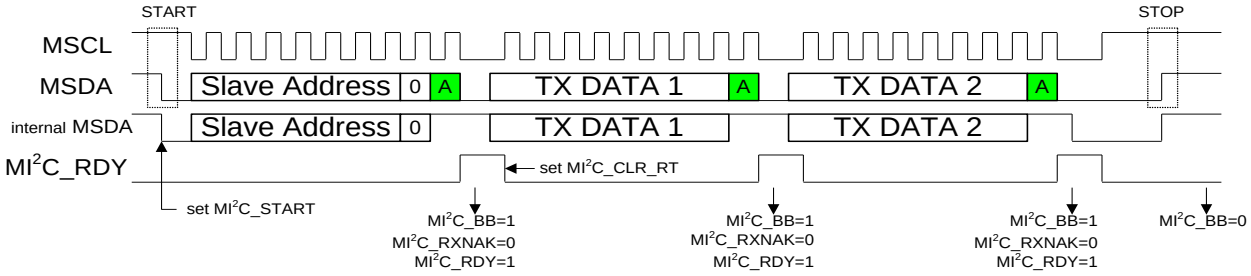
-: unimplemented.

If the firmware processing time is slower than the time of I²C receiving 9 bits, then the firmware must set MI²C_WAIT enabling WT56F248/232 to pull SCL low after the 9th bit.

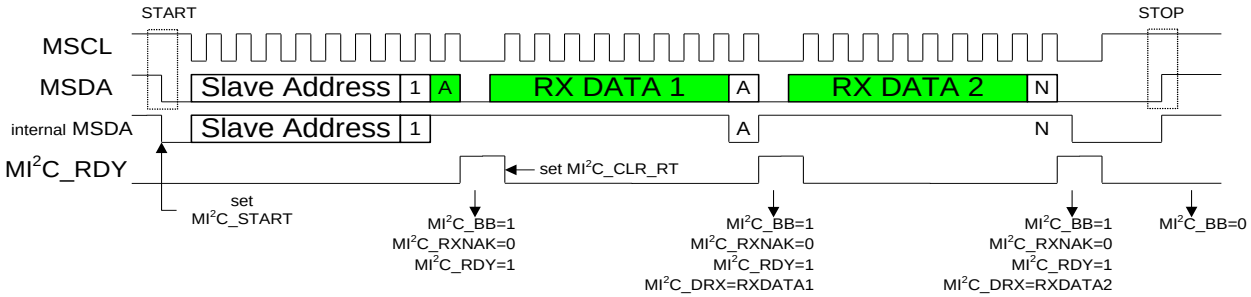


WT56F248/232 Master/Slave I²C Data Flow

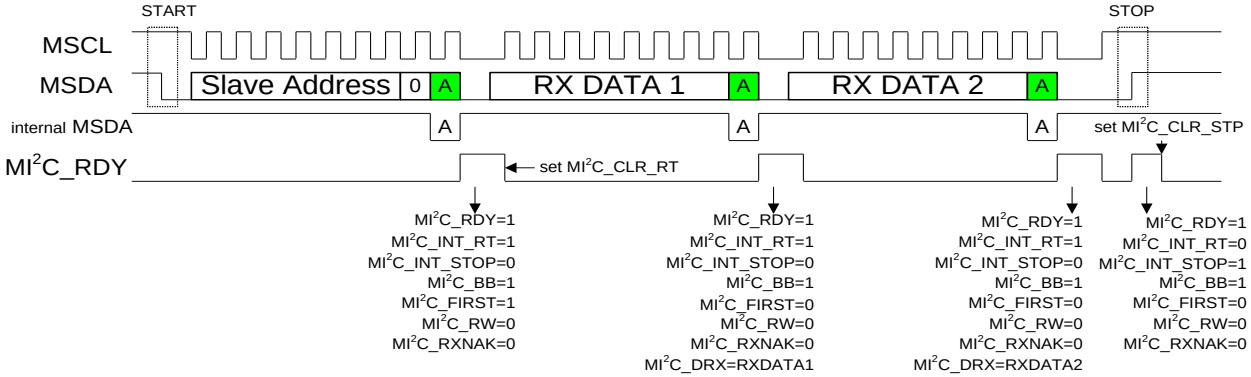
(1) Master write mode :



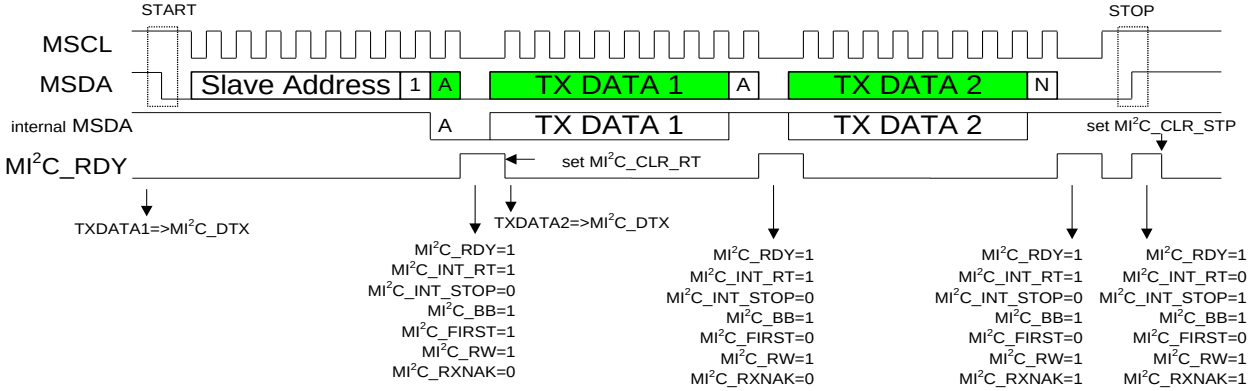
(2) Master read mode :



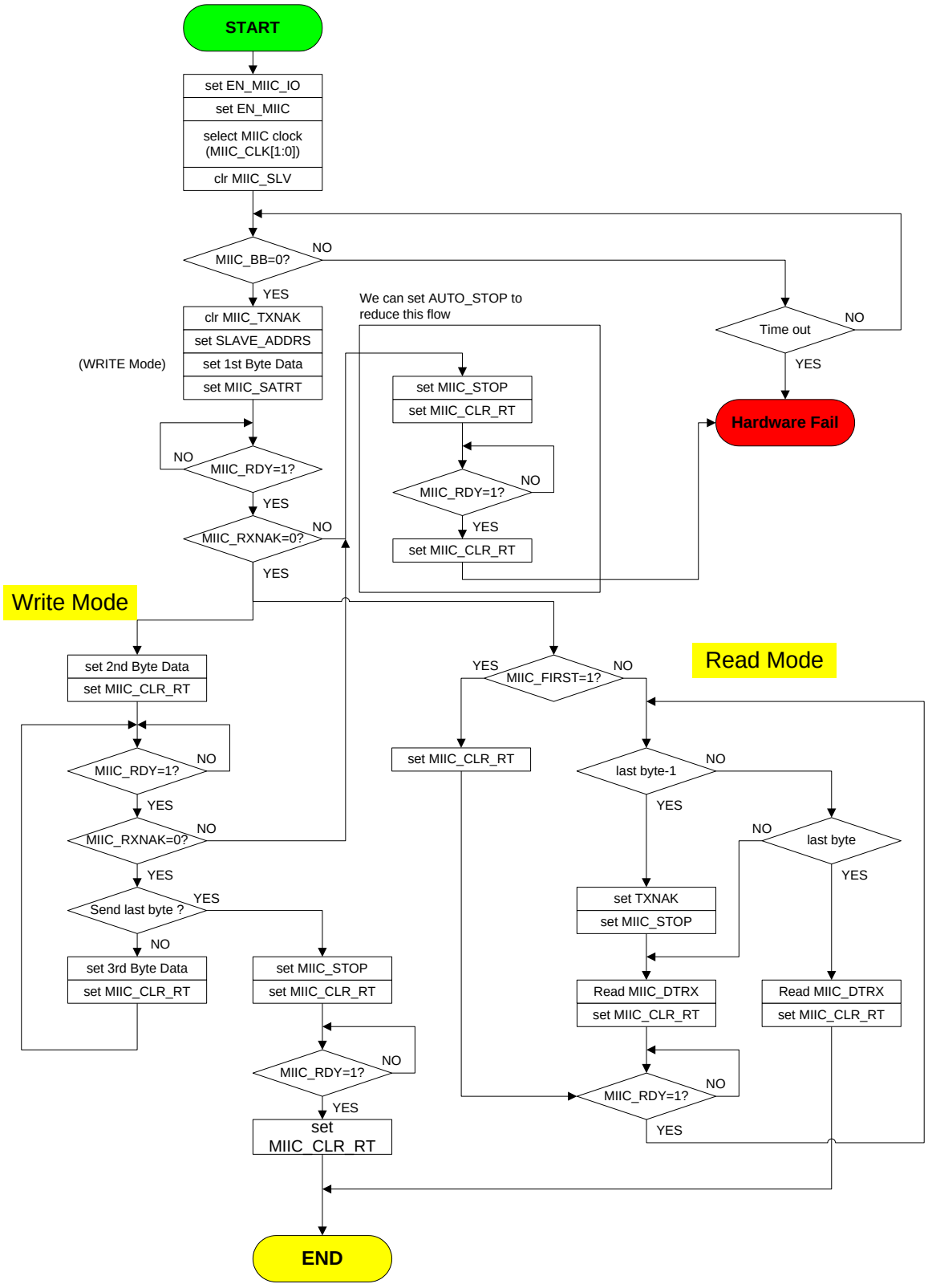
(3) Slave write mode :



(4) Slave read mode :



WT56F248/232 Master/Slave I²C Data Flow



6.12 Enhanced Timer/Counter

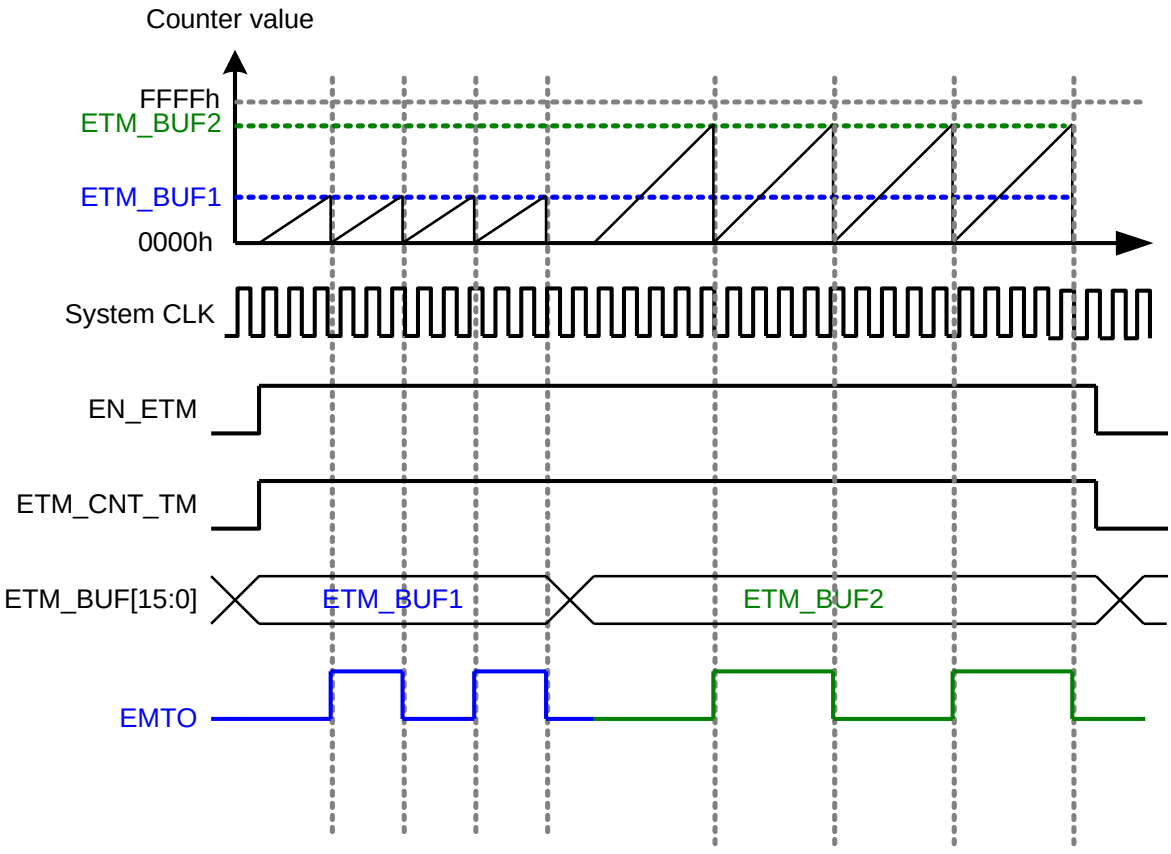
The clock sources of enhanced Timer/Counter are from internal or external clock, and it is determined by register.

The Enhanced Timer/Counter has two operation modes: 1. Compare mode. 2. Capture mode. Furthermore there are three types of Capture Match condition for selection: High-level, Low-level, and Period of Capture mode.

1. Compare mode:

The Enhanced Timer/Counter contains one 16-bit Counter and one 16-bit enhanced Buffer (ETM_BUF[15:0]). When enable the Enhanced Timer/Counter (EN_ETM = 1) and set as the compare mode (ETM_CNT_TM = 1), the counter will start counts according to the clock sources, and an interrupt will occur once the data of the counter matches the data of the enhanced Buffer. Each match will output the trigger of ETMO (general-purpose I/O port A7) and clear the counter value of the internal 16-bit Counter. Please refer to the figure below.

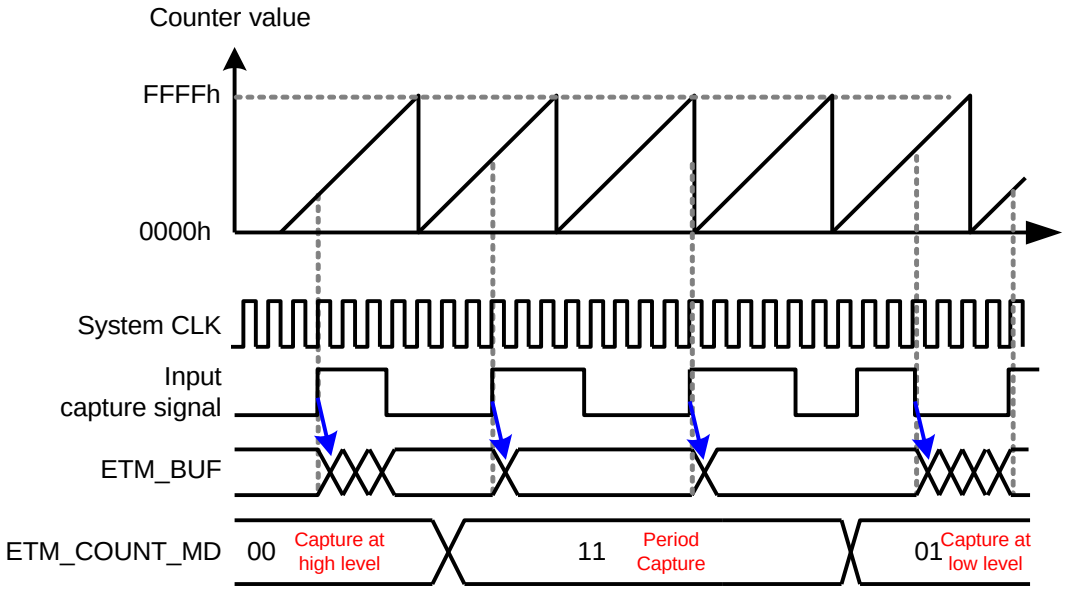
Compare mode operation flow:



2. Capture mode

If the Enhanced Timer/Counter is set as the Capture mode (ETM_CNT_TM = 0), and it is enabled (EN_ETM = 1), the capture operation starts. When the input status changes then match with the setting capture condition, the internal 16-bit counter will be cleared and restarts counting, then reload the counter value into 16-bit Buffer (ETM_BUF[15:0]) automatically. At the same time, the software can read the counter value from the Enhanced Timer/Counter Data Buffer Register (register B3H & B4H), and a capture interrupt, capture flag and output ETMO may be generated. Please refer to the figure below.

Capture mode operation flow:



Enhanced Timer/Counter Control Register 1 ETM_CTL1(XFR: 0xB0) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	RW	R/W	R/W	R/W
Name	EN_ETM	ETM_CNT_TM	ETM_CLK_PSCAL[1:0]		ETM_CLK_SEL	ETM_EXCLK_SEL[1:0]		ETM_CLK_DIV12

Bit Number	Bit Mnemonic	Description
7	EN_ETM	1: Enable Enhanced Timer/Counter
6	ETM_CNT_TM	1: Compare mode (SOURCE clock = 12 MHz) 0: Capture mode
5-4	ETM_CLK_PSCAL[1:0]	Set clock source prescalers of the internal 16-bit Counter 00: Enhanced Timer/Counter clock source = SOURCE clock/1 01: Enhanced Timer/Counter clock source = SOURCE clock/4 10: Enhanced Timer/Counter clock source = SOURCE clock/8 **11: Choose Timer/Counter clock base SOURCE clock/16 or SOURCE clock/12** **(ETM_CLK_DIV12: 0 -> SOURCE clock/16;** **ETM_CLK_DIV12: 1 -> SOURCE clock /12)**

Bit Number	Bit Mnemonic	Description
3	ETM_CLK_SEL	Set Enhanced Timer/Counter clock source 1: external clock source (can select the input clock source by ETM_EXCLK_SEL [1:0]) 0: internal clock source (SOURCE clock)
2-1	ETM_EXCLK_SEL[1:0]	Set Enhanced Timer/Counter input external clock source channel 00: GPIOE6 (set GPIOE6DH as ETMI, GPE6_FUN_SLT[1:0] = 10) 01: ACOMP_TGATE_O (internal signal, refer to section 6.15) 10: GPIOF2 (set GPIOF2DH as T2CAP, GPF2_FUN_SLT[1:0] = 10) 11: GPIOF1 (set GPIOF1DH as T2 input, GPF1_FUN_SLT[1:0] = 01)
0	ETM_CLK_DIV12	1: SOURCE clock/12 0: SOURCE clock/16

-: unimplemented.

Enhanced Timer/counter Control Register 2 ETM_CTL2 (XFR: 0xB1) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	-	-	RW	R/W	R/W	R/W
Name	ETM_IN_SOURCE[1:0]		Reserved		ETM_IN_PSCAL[1:0]		ETM_COUNT_MD[1:0]	

Bit Number	Bit Mnemonic	Description
7-6	ETM_IN_SOURCE[1:0]	Set Enhanced Timer/Counter input compare or capture channel 00: GPIOE6 (set GPIOE6DH as ETMI, GPE6_FUN_SLT[1:0] = 10) 01: ACOMP_TGATE_O (internal signal, refer to section 6.15) 10: GPIOF2 (set GPIOF2DH as T2CAP, GPF2_FUN_SLT[1:0] = 10) 11: GPIOF1 (set GPIOF1DH as T2 input, GPF1_FUN_SLT[1:0] = 01)
5-4	Reserved	-
3-2	ETM_IN_PSCAL[1:0]	Set input channel period prescaler 00: input period/1 01: input period/4 10: input period/8 11: input period/16
1-0	ETM_COUNT_MD[1:0]	Capture counting mode selection 00: capture the interval of high level 01: capture the interval of low level 1x: capture the interval period (based on the setting ETM_IN_PSCAL[1:0] to capture)

-: unimplemented.

Enhanced Timer/Counter Interrupt Register ETM_INT (XFR: 0xB2) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R	R	R	-
Name	EN_CAPINT	EN_OVRINT	EN_CMPINT	CLR_FLAG	CAPF	OVRF	CPMF	Reserved

Bit Number	Bit Mnemonic	Description
7	EN_CAPINT	1: Enable input capture interrupt 0: Disable input capture interrupt
6	EN_OVRINT	1: Enable overflow interrupt 0: Disable overflow interrupt

Bit Number	Bit Mnemonic	Description
5	EN_CMPINT	1: Enable Compare Match Interrupt 0: Disable Compare Match Interrupt
4	CLR_FLAG	1: Clear all Enhanced Timer/Counter flags
3	CAPF	Input capture flag
2	OVRF	Overflow flag When an overflow occurred in internal 16-bit counter, OVRF = 1
1	CPMF	Compare match flag When internal 16-bit counter has the same value as ETM_BUF, CPMF = 1
0	Reserved	-

-: unimplemented.

Enhanced Timer/Counter Data Buffer Low Bytes Register ETM_BUF[7:0] (XFR: 0xB3) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	ETM_BUF[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	ETM_BUF[7:0]	Paired with ETM_BUF[15:8] to form a 16-bit counter value Read: In Capture mode, the counter value of the captured input signal Write: In Compare mode, as the compare value to compare with the internal 16-bit counter

Enhanced Timer/Counter Data Buffer High Bytes Register ETM_BUF [15:8] (XFR: 0xB4) **Reset Value: 80h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	ETM_BUF[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	ETM_BUF[15:8]	Paired with ETM_BUF[7:0] to form a 16-bit counter value Read: In Capture mode, the counter value of the captured input signal Write: In Compare mode, as the compare value to compare with the internal 16-bit counter

Note: In Capture mode, ETM_BUF[15:8] and ETM_BUF[7:0] form a 16-bit counter value, and the counter value should be incremented by one to be the actual counter value in application.

Explanation 1:

Due to the internal source goes through the filter, the pulse width of input signal high level and low level must be greater than the width of two SYSTEM Clocks.

Explanation 2:

ETM_IN_PSCAL[3:2] = 00: Select Capture Input Source 1 cycle, then the Capture effective Resolution is as below:

If Source Clock = 12 MHz, (1/12 MHz)/1 = 83.333 ns;

If Source Clock = 24 MHz, (1/24 MHz)/1 = 41.666 ns.

ETM_IN_PSCAL[3:2] = 11: Select Capture Input Source 16 cycles, then the Capture effective Resolution is as below:

If Source Clock = 12 MHz, (1/12 MHz)/16 = 5.208 ns;

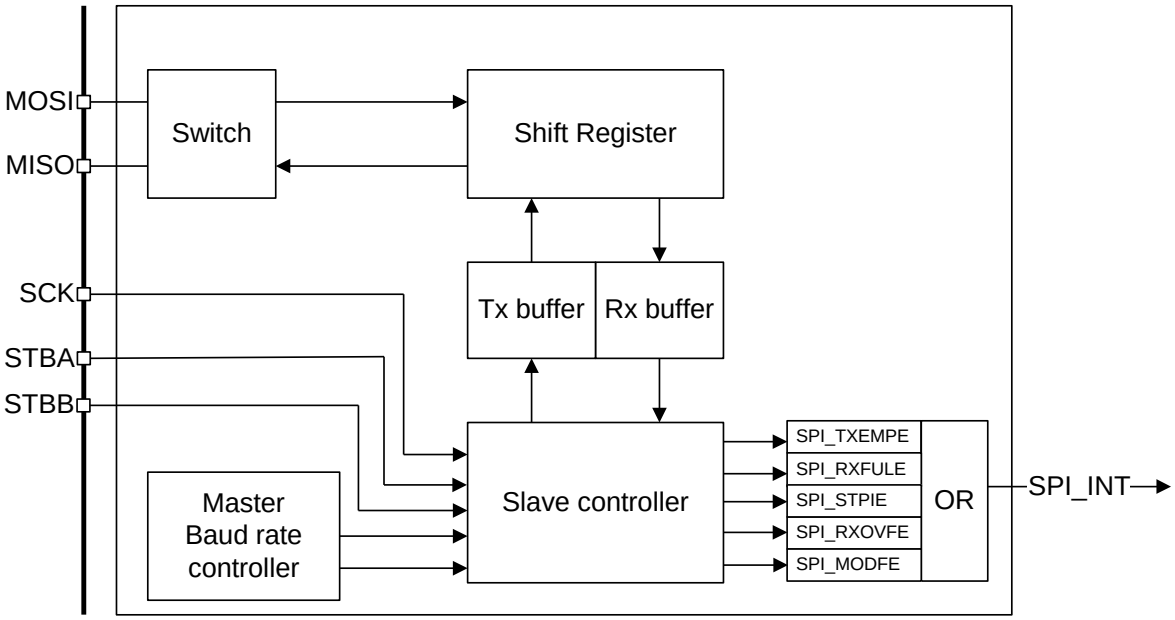
If Source Clock = 24 MHz, (1/24 MHz)/16 = 2.604 ns.

When select Capture 16 cycles allow the enhanced Timer/Counter to get more significant digits, to reduce capture error.

6.13 Serial Peripheral Interface (SPI)

SPI is a synchronous serial interface, allows master to communicate with slave, supports full duplex data transmission, and also supports 3-wire or 4-wire communication.

- SPI supports: Master and Slave mode
- Transmitted serial data can select LSB or MSB being transmitted first
- SPI serial interface transmission speed, frequency range: 6 MHz ~ 23.4375 kHz (Bit Rate)

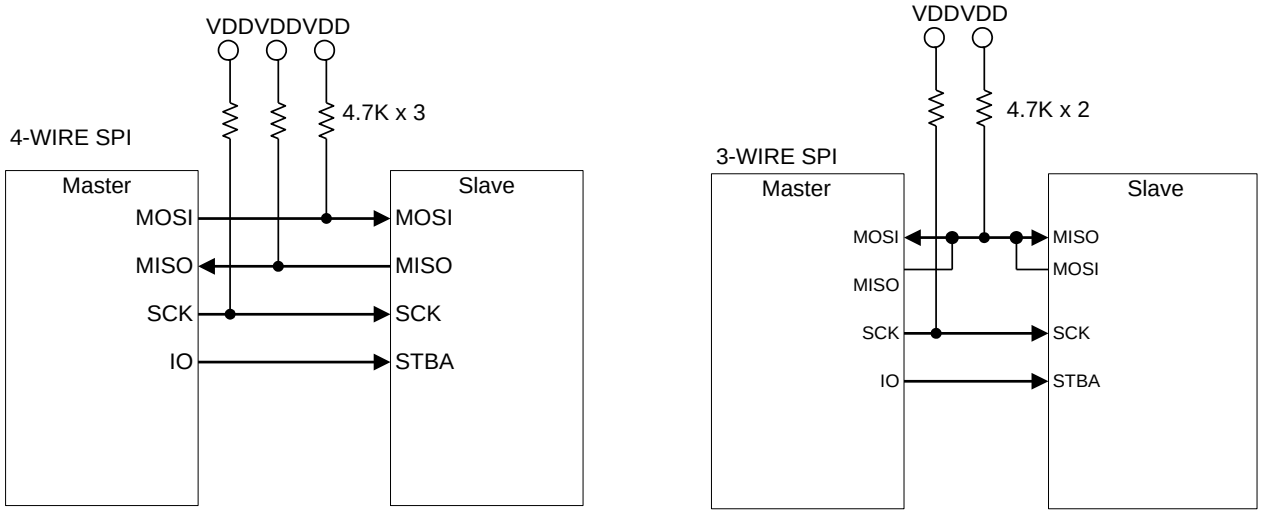


SPI communication uses four pins, as described below.
MOSI: In Master mode data output; in slave mode data input.
MISO: In Master mode data input; in slave mode data output.
SCK: In Master mode clock output; in slave mode clock input for data synchronization.
STBA, STBB: In Master mode as output; in slave mode as input.
In Master mode, as the I/O port to enable Slave:
STBx = 0: Master enables Slave
STBx = 1: Master disables Slave

When use the SPI serial interface, the SPI related pins must be set as output or input status by software, as illustrated below:

4-wire SPI	Master mode	Slave mode	Remarks
MOSI (GPIOF1/GPIOA0)	Output	Input	Path A: GPIOF1 Path B: GPIOA0
MISO (GPIOA3)	Input	Output	
SCK (GPIOE7)	Output	Input	
STB (GPIOF2/GPIOA6)	Output	Input	Path A: GPIOF2 Path B: GPIOA6

4-wire and 3-wire SPI connection diagram:



SPI Control Register 1 SPI_CTL1 (XFR: 0xC0) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	R/W	-	-
Name	SPI_EN	SPI_MASTER	SPI_CPOL	SPI_CPHA	Reserved	SPI_LSBFE	Reserved	

Bit Number	Bit Mnemonic	Description
7	SPI_EN	1: Enable SPI module 0: Disable SPI module
6	SPI_MASTER	SPI Master/Slave mode selection 1: SPI as Master mode 0: SPI as Slave mode
5	SPI_CPOL	SPI Clock Polarity bit selection 1: Active-low clock selection 0: Active-high clock selection
4	SPI_CPHA	SPI Clock Phase bit selection 1: sampling data at even edge of input SPI clock 0: sampling data at odd edge of input SPI clock
3	Reserved	-
2	SPI_LSBFE	LSB-First Enable 1: Data is transferred LSB bit first 0: Data is transferred MSB bit first
1-0	Reserved	-

-: unimplemented.

***SPI serial interface modes are composed of SPI_CPOL and SPI_CPHA, and are classified into four modes as listed below.**

SPI_CPOL	SPI_CPHA	Receive data by	Transmit data by	SPI Mode
0	0	Positive-edge trigger	Negative-edge trigger	0
0	1	Negative-edge trigger	Positive-edge trigger	1
1	0	Negative-edge trigger	Negative-edge trigger	2

SPI_CPOL	SPI_CPHA	Receive data by	Transmit data by	SPI Mode
1	0	Positive-edge trigger	Positive-edge trigger	3

*** Transmit and Receive methods can also refer to "SPI Mode Timing" section that will be described later.**

SPI Control Register 2 SPI_CTL2 (XFR: 0xC1) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	-	-	-
Name	SPI_RXONLY	SPI_DFBYP	SPI_DLY[1:0]		Reserved			

Bit Number	Bit Mnemonic	Description
7	SPI_RXONLY	SPI Receive Enable Bit (Master mode use only) 1: Enable SPI Receive mode
6	SPI_DFBYP	Input Digital Filter Bypass Enable Bit (Slave mode use only) 1: Enable Digital Filter
5-4	SPI_DLY[1:0]	Master SPI byte delay control 00: No delay 01: delay 1 byte 10: delay 2 bytes 11: delay 3 bytes
3-0	Reserved	-

-: unimplemented.

SPI Interrupt Control Register SPI_INT (XFR: 0xC2) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	-	-	-
Name	SPI_TXEMPE	SPI_RXFULE	SPI_STPIE	SPI_RXOVFE	SPI_MODFE	Reserved		

Bit Number	Bit Mnemonic	Description
7	SPI_TXEMPE	1: Enable SPI Tx data buffer empty interrupt
6	SPI_RXFULE	1: Enable SPI Rx data buffer full interrupt
5	SPI_STPIE	1: Enable SPI Tx sequence finish interrupt
4	SPI_RXOVFE	1: Enable SPI Rx data buffer overflow interrupt
3	SPI_MODFE	1: Enable SPI mode fault Interrupt (Slave mode only)
2-0	Reserved	-

-: unimplemented.

SPI Interrupt Clear Register SPI_CLR (XFR: 0xC3) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	-	-	-	-
Name	CLR_TXEMP	CLR_RXFUL	CLR_STPIF	CLR_RXOVF	Reserved			

Bit Number	Bit Mnemonic	Description
7	CLR_TXEMP	1: Clear SPI Tx data buffer empty interrupt flag

Bit Number	Bit Mnemonic	Description
6	CLR_RXFUL	1: Clear SPI Rx data buffer interrupt flag
5	CLR_STPIF	1: Clear SPI sequence full finish interrupt flag
4	CLR_RXOVF	1: Clear SPI Rx data buffer overflow flag
3-0	Reserved	-

-: unimplemented.

SPI Flag Register SPI_FLG (XFR: 0xC4) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	-	-
Name	SPI_TXEMP	SPI_RXFUL	SPI_STPIF	SPI_RXOVF	SPI_MODF	SPI_BUSY	Reserved	

Bit Number	Bit Mnemonic	Description
7	SPI_TXEMP	SPI transmit data buffer empty flag *1 1: SPI Tx data buffer is empty
6	SPI_RXFUL	SPI receive data buffer full flag 1: SPI Rx data buffer is full
5	SPI_STPIF	SPI Transmit/Receive data finish flag (SS pin goes high) 1: SPI Tx/Rx finish
4	SPI_RXOVF	SPI Rx data buffer overflow flag *2 1: SPI receive data buffer overflows
3	SPI_MODF	SPI mode failure status flag (only allowed in Slave mode) *3 1: SPI mode failure
2	SPI_BUSY	SPI Busy status flag *4 1: SPI busy status
1-0	Reserved	-

-: unimplemented.

*1. The firmware must confirm that only when SPI_TXEMP = 1, then the next data is allowed to be written into SPI Transmit Buffer Register (SPI_RXBUF[7:0]).

*2. The SPI_RXOVF flag can be cleared by reading SPI Receive Buffer Register (SPI_RXBUF[7:0]).

*3. The SPI_MODF flag can be cleared by enabling SPI serial interface module.

*4. SPI_BUSY flag is the status of the WT56F248/232 internal pin, and it can monitor if SPI is finished or not.

SPI Bit Rate Setting Register SPI_BRS[7:0] (XFR: 0xC5) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	SPI_BRS[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	SPI_BRS[7:0]	SPI Bit rate selection (SPI maximum clock = mcu_clk/2) SPI Bit rate = mcu_clk/(SPI_BRS[7:0]+1) x 2 If mcu_clk = 12 MHz, SPI_BRS[7:0] = 0, SPI Bit Rate is 6 MHz SPI_BRS[7:0] = 1, SPI Bit Rate is 3 MHz …

Bit Number	Bit Mnemonic	Description
		SPI_BRS[7:0] = 255, SPI Bit Rate is 23.4375 kHz

SPI Transmit Buffer Register SPI_TXBUF[7:0] (XFR: 0xC6) **Reset Value: FFh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	SPI_TXBUF[7:0]							

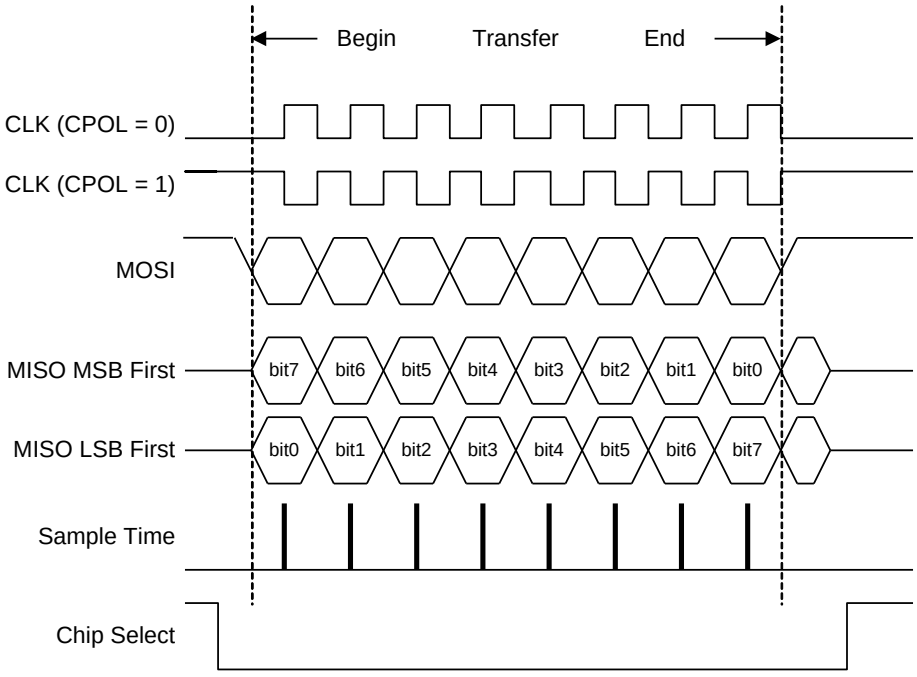
Bit Number	Bit Mnemonic	Description
7-0	SPI_TXBUF[7:0]	SPI Transmit Data Buffer

SPI Receive Buffer Register SPI_RXBUF[7:0] (XFR: 0xC7) **Reset Value: 00h**

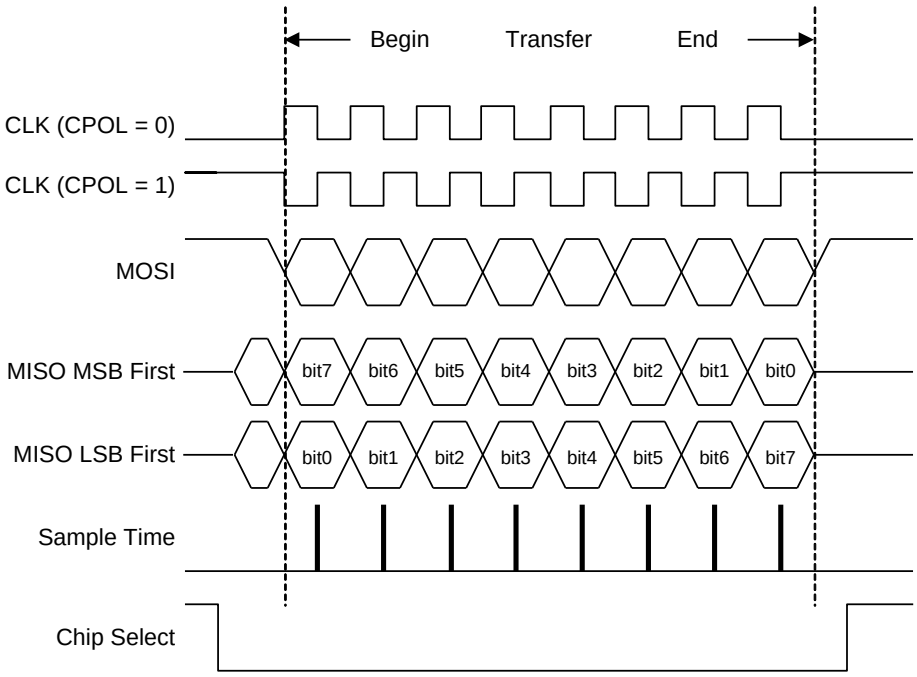
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	SPI_RXBUF[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	SPI_RXBUF[7:0]	SPI Receive Data Buffer

SPI Mode Timing



(CPHA = 0)



(CPHA = 1)

6.14 Analog/Digital Converter (ADC)

WT56F248/232 has a built-in 16-channel 12-bit Analog/Digital Converter, and it also provides four conversion modes (Single, Continuous, Voltage Compare, and Timer Auto mode) and four conversion rate (1 MHz, 500 kHz, 125 kHz, and 31.25 kHz) for selection.

- The conversion time of A/D Converter is 16us (sampled time 4 us + conversion time 12 us) based on the conversion rate of 1 MHz
- Reference Voltage sources VREF have three selections: Power Voltage VDD, Built-in voltage reference VBGAP, and External voltage reference VREF

Note: In this mode, the converting frequency can only select 31.25 kHz (ADC_CLK_SEL[1:0] = 11) to get the correct converting result if the reference voltage select built-in VBGAP.

Single Mode:

Turn on the A/D converter power (XFR: 0xD0 ADC_CTL, and ADC_PD = 0), and set the ADC_SINGLE_CVT = 1, then the A/D conversion starts. When ADC_SINGLE_CVT = 0, the conversion is finished. When conversion is completed, the conversion data will be updated and an interrupt will generate (ADFINSH_FLG = 1). If ADC convert finish Interrupt is enabled (EN_ADFINSH_INT = 1), the ADC interrupt will generate.

Continuous Mode:

If activate continuous convert control bit XFR: 0xD0 ADC_CTL and ADC_CNTNU_CVT = 1, the system will enter the Continuous Conversion Mode. When conversion is completed, the conversion data will be updated and an interrupt will generate (ADFINSH_FLG = 1). If ADC convert finish Interrupt is enabled (EN_ADFINSH_INT = 1), the ADC interrupt will generate.

Voltage Compare Mode:

When turn on the A/D converter power (XFR: 0xD0 ADC_CTL, and ADC Control Register ADC_PD = 0), and activate the Compare function (EN_ADC_CMP = 1), the conversion data of Analog input compare 12-bit setting of XFR: 0xD4 & 0xD5 (ADC_CMP_V). When the corresponding digital value of the voltage analog input is greater than (ADC_BIG = 0) or smaller than (ADC_BIG = 1) the setting value of ADC_CMP_V register, the ADC interrupt will occur. The Voltage Compare function of A/D Converter module works as a wakeup source. In addition, working together with XFR: 0xD1 ADC_SEL & ADCMP_TM, it can define ADC turn on time for power-saving purpose.

Timer Auto Mode:

When turn on the ADC_AUTO_CVT and work together with the setting of Watch Timer, each Timer event will automatically activate ADC for one-time conversion.

ADC Control Register ADC_CTL (XFR: 0xD0) **Reset Value: 80h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	-	R/W
Name	ADC_PD	ADC_SINGLE_CVT	ADC_CNTNU_CVT	ADC_AUTO_CVT	EN_ADC_CMP	EN_ADC_FLT	Reserved	ADC_BIG

Bit Number	Bit Mnemonic	Description
7	ADC_PD	Analog/Digital Converter Power Control 1: turn off ADC power 0: turn on ADC power
6	ADC_SINGLE_CVT	ADC start convert bit (single convert mode) 1: ADC start convert 1 => 0: convert finished (hardware will be auto-cleared as “0”)
5	ADC_CNTNU_CVT	1: Enable ADC continuous convert (continuous convert mode) 0: Disable ADC continuous convert
4	ADC_AUTO_CVT	1: Enable ADC auto convert one time based on Watch Timer event WTMR_SLT[2:0] (Timer Compare mode)
3	EN_ADC_CMP	1: Enable ADC compare mode (Voltage compare mode)
2	EN_ADC_FLT	1: Enable ADC filter (need to wait for 332 nsec) 0: Disable filter function
1	Reserved	-
0	ADC_BIG	ADC data compare flag 1: the data set when Vin < ADC_CMP_V[11:0] 0: the data set when Vin > ADC_CMP_V[11:0] Vin: the channel select by EN_AD[3:0]

Note: Only one converting mode is allowed to enable the ADC at the same time, otherwise ADC may work abnormally.

ADC Setting Control Register ADC_SEL (XFR: 0xD1) **Reset Value: 40h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	-	-	-	R/W	R/W
Name	ADC_CLK_SEL[1:0]		ADCMP_TM	Reserved			ADC_VREF_SEL[1:0]	

Bit Number	Bit Mnemonic	Description
7-6	ADC_CLK_SEL[1:0]	ADC convert time clock base, when MCU clock selects 12 MHz 00: 1 MHz (MCU_Clock /12) 01: 500 kHz (MCU_Clock /24) 10: 125 kHz (MCU_Clock /96) 11: 31.25 kHz (MCU_Clock /384)
5	ADCMP_TM	1: ADC compare time from watch timer clock every 32u seconds for power-saving purpose 0: ADC always compare time
4-2	Reserved	-
1-0	ADC_VREF_SEL[1:0]	ADC reference voltage selection 00: from VDD 01: from VREF pin 1x: from internal reference voltage BGAP (Bandgap) BGAP can set two voltage 1.22V or 2.44V, please refer to register “GP_VOL_SLT”

Note: Internal reference voltage Bandgap is not calibrated out of the factory, and will be affected by the impact of temperature and supply voltage. The actual voltage value can be read by register. Please refer to the section below and 7.6 & 7.7 Electrical Characteristics.

VBGAP Voltage stored address:

External Memory Address	Description
E04H[3:0]	Record internal Bandgap voltage low bytes = ADC[3:0]
E05H[7:0]	Record internal Bandgap voltage high bytes = ADC[11:4]

VBGAP Voltage formula: VBGAP = (5 * ADC[11:0]) / 4096

Examples:

E04H[3:0] = 0x08
E05H[7:0] = 0x3E
VBGAP = (5 * 0x3E8) / 4096 = 1.221V

ADC Interrupt Control Register ADC_INT (XFR: 0xD2) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	-	-	R	R	R	-
Name	EN_ADCMP_INT	EN_ADFINSH_INT	Reserved		ADCMP_FLG	ADFINSH_FLG	ADCMP_FLG	Reserved

Bit Number	Bit Mnemonic	Description
7	EN_ADCMP_INT	1: Enable ADC Compare Interrupt 0: Disable ADC Compare Interrupt
6	EN_ADFINSH_INT	1: Enable ADC Convert Finish Interrupt 0: Disable ADC Convert Finish Interrupt
5-4	Reserved	-
3	ADCMP_FLG	ADC Compare Mode Flag. If the condition selected by ADC_BIG bit in ADC Control Register is met, ADCMP_FLG = 1.
2	ADFINSH_FLG	ADC Finish Interrupt Flag (If the ADC finished convert in single, continuous or timer mode, ADFINSH_FLG = 1)
1	ADCMP_FLG	1: Vin > ADC_WK_V 0: Vin < ADC_WK_V
0	Reserved	-

-: unimplemented.

Note: When read AD_DATA[11:0], the hardware will auto clear the ADCMP_FLG and ADFINSH_FLG flag.

ADC Channel Control Register ADC_ENCH (XFR: 0xD3) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				EN_AD[3:0]			

Bit Number	Bit Mnemonic	Description
7-4	Reserved	-
3-0	EN_AD[3:0]	Analog/Digital Channel Selection 0000: Select Channel CH0

Bit Number	Bit Mnemonic	Description
		0001: Select Channel CH1 0010: Select Channel CH2 0011: Select Channel CH3 0100: Select Channel CH4 0101: Select Channel CH5 0110: Select Channel CH6 0111: Select Channel CH7 1000: Select Channel CH8 1001: Select Channel CH9 1010: Select Channel CH10 1011: Select Channel CH11 1100: Select Channel CH12 1101: Select Channel CH13 1110: Select Channel CH14 1111: Select Channel CH15

-: unimplemented.

ADC Voltage Compare Data High Bytes Register ADC_CMP_V[11:4] (XFR: 0xD4) Reset Value: 80h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
N**ame**	ADC_CMP_V[11:4]							

Bit Number	Bit Mnemonic	Description
7-0	ADC_CMP_V[11:4]	ADC_CMP_V[11:4] Compare Voltage Setting, paired with ADC_CMP_V[3:0] to form a 12-bit data

ADC Voltage Compare Data Low Bytes Register ADC_CMP_V[3:0] (XFR: 0xD5) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
N**ame**	Reserved				ADC_CMP_V[3:0]			

Bit Number	Bit Mnemonic	Description
7-4	Reserved	-
3-0	ADC_CMP_V[3:0]	ADC_CMP_V[3:0] Compare Voltage setting, paired with ADC_CMP_V[11:4] to form a 12-bit data

-: unimplemented.

ADC Converted Data High Bytes Register AD_DATA[11:4] (XFR: 0xD6) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	AD_DATA[11:4]							

Bit Number	Bit Mnemonic	Description
7-0	AD_DATA[11:4]	AD_DATA[11:4] converted data setting, paired with AD_DATA[3:0] to form a 12-bit data

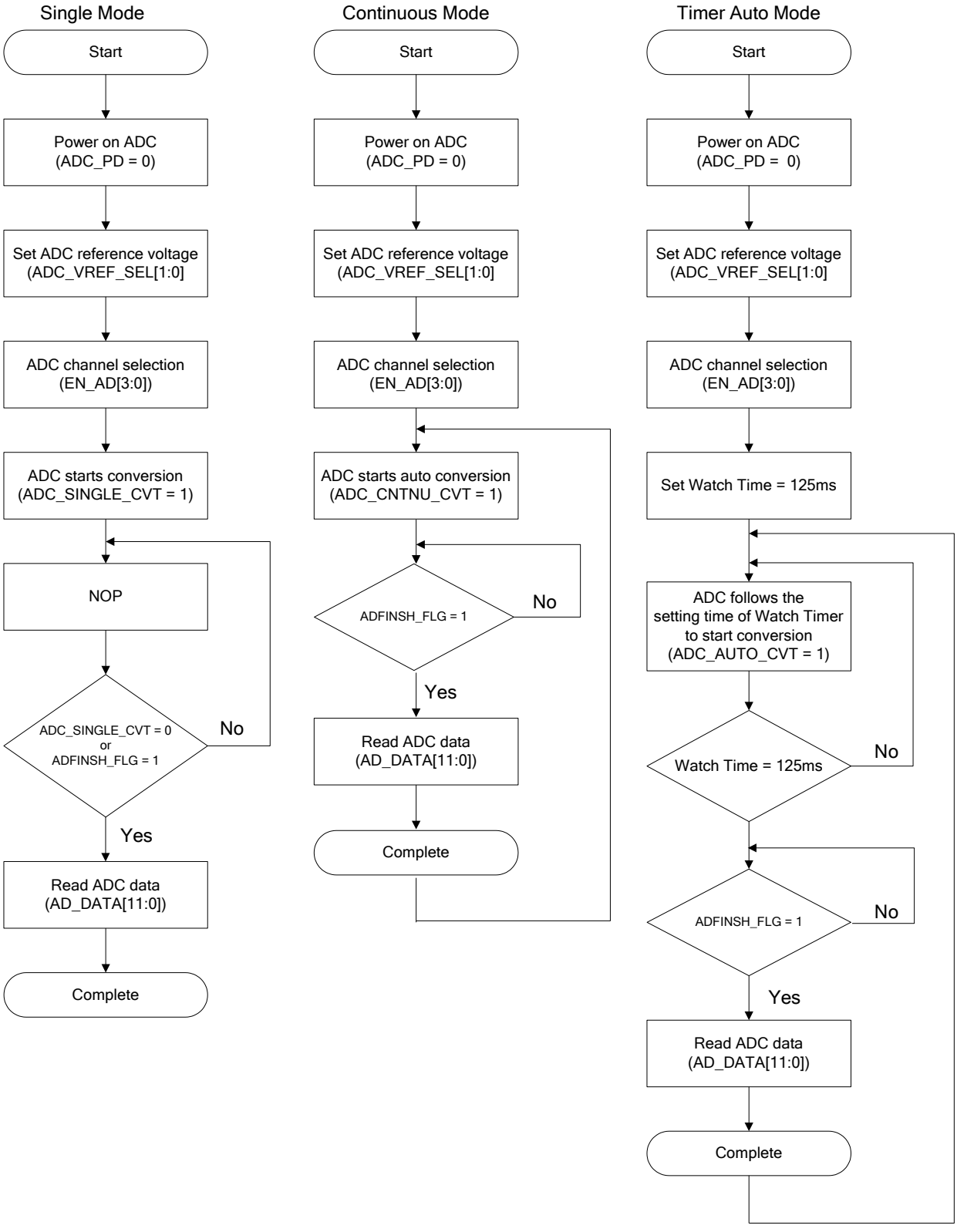
ADC Converted Data Low Bytes Register AD_DATA[3:0] (XFR: 0xD7) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R	R	R	R
Name	Reserved				AD_DATA[3:0]			

Bit Number	Bit Mnemonic	Description
7-4	Reserved	-
3-0	AD_DATA[3:0]	AD_DATA[3:0] converted data setting, paired with AD_DATA[11:4] to form a 12-bit data

-: unimplemented.

The setting of Enabling Analog/Digital Converter converted Data procedure:



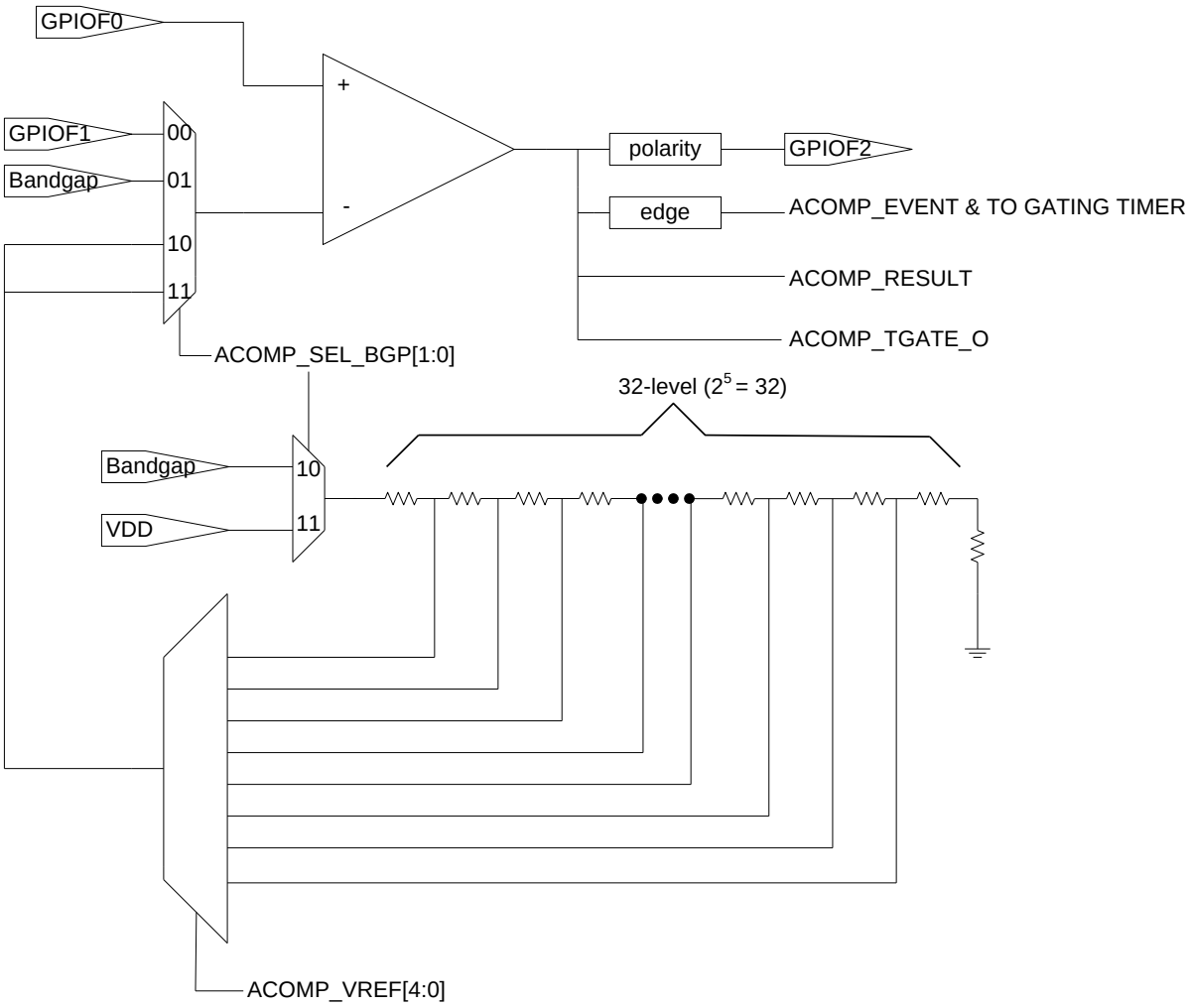
6.15 Comparator

WT56F248/232 built-in one Analog Voltage Comparator with features as listed below.

- Comparator can be enabled or disabled individually.
- The comparator reference voltage is determined by the corresponding Comparator Control Register (ACOMP_VREF).
- Either the positive-edge or negative-edge of the comparator can generate Interrupt.
- Embedded with comparator capture function (refer to section 6.12).

When the comparator function is enabled (XFR: 0xDA, ACOMP_PD = 0), the Comparator can compare input (GPIOF0 = CMPP) with the comparator reference voltage (GPIOF1 = CMPN). Then three methods of performing are listed below:

1. Interrupt
2. Event Flag (GPIOF2)
3. Via the Enhanced Timer to perform Gating Timer function



Comparator Control Register ACOMP_CTL(XFR: 0xDA) **Reset Value: E0h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	-	-	-
Name	ACOMP_PD	ACOMP_SEL_BGP[1:0]		ACOMP_OUT_INV	ACOMP_TGATE	Reserved		

Bit Number	Bit Mnemonic	Description
7	ACOMP_PD	1: Power down Comparator 0: Power on Comparator
6-5	ACOMP_SEL_BGP[1:0]	Comparator CMPN input selection 00: Select GPIOF1 input COMN 01: Select Bandgap input COMN 10: Select nxBGP/32 input COMN 11: Select nxVDD/32 input COMN When select $\frac{n}{32}BGP$ or $\frac{n}{32}VDD$ as input COMN, which can work together with Comparator Reference Voltage Register (0xDC) to provide 32-level reference voltage sources
4	ACOMP_OUT_INV	1: Invert ACOMP_RESULT output 0: Did not invert ACOMP_RESULT output
3	ACOMP_TGATE	1: Comparator output gating signal to enhanced timer/counter to calculate comparator H/L time 0: Comparator didn't output gating signal to enhanced timer/counter
2-0	Reserved	-

-: unimplemented.

Note: Internal reference voltage Bandgap is not calibrated out of the factory, and will be affected by the impact of temperature and supply voltage. Please refer to section 6.14 for the actual voltage value.

Comparator Flag Register ACOMP_FLG (XFR: 0xDB) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R/W	R	R/W	-	-	-	-
Name	ACOMP_RESULT	ACOMP_EVENT_EDGE	ACOMP_EVENT	CLR_ACOMP_EVENT	Reserved			

Bit Number	Bit Mnemonic	Description
7	ACOMP_RESULT	1: Comparator CMPP voltage > CMPN voltage 0: Comparator CMPP voltage < CMPN voltage (When ACOMP_PD = 1, **ACOMP_RESULT = 0**)
6	ACOMP_EVENT_EDGE	1: Comparator CMPP voltage < CMPN voltage trigger Interrupt 0: Comparator CMPP voltage > CMPN voltage trigger Interrupt
5	ACOMP_EVENT	Comparator Trigger Flag 1: Comparator trigger occurred 0: Comparator trigger not occurred
4	CLR_ACOMP_EVENT	1: Clear Comparator Trigger Flag 0: no action
3-0	Reserved	-

-: unimplemented.

Comparator Reference Voltage Register ACOMP_VREF[4:0] (XFR: 0xDC) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	R/W	R/W	R/W	R/W	R/W
Name	Reserved			ACOMP_VREF[4:0]				

Bit Number	Bit Mnemonic	Description
7-5	Reserved	-
4-0	ACOMP_VREF[4:0]	Comparator Reference Voltage input CMPN, CMPN reference voltage = ACOMP_VREF[4:0] *(VDD-VSS)/32 = $\frac{n}{32}$VDD or ACOMP_VREF[4:0] * $V_{Bandgap}$ /32 = $\frac{n}{32}$BGP

-: unimplemented.

Comparator Pin Enable Register ACOMP_IOCTL (XFR: 0xDD) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	-	-	-	-	-	-
Name	ACOMP_CMPP_IO	ACOMP_CMPN_IO	Reserved					

Bit Number	Bit Mnemonic	Description
7	ACOMP_CMPP_IO	1: set GPIOF0 as comparator CMPP pin
6	ACOMP_CMPN_IO	1: set GPIOF1 as comparator CMPN pin
5-0	Reserved	-

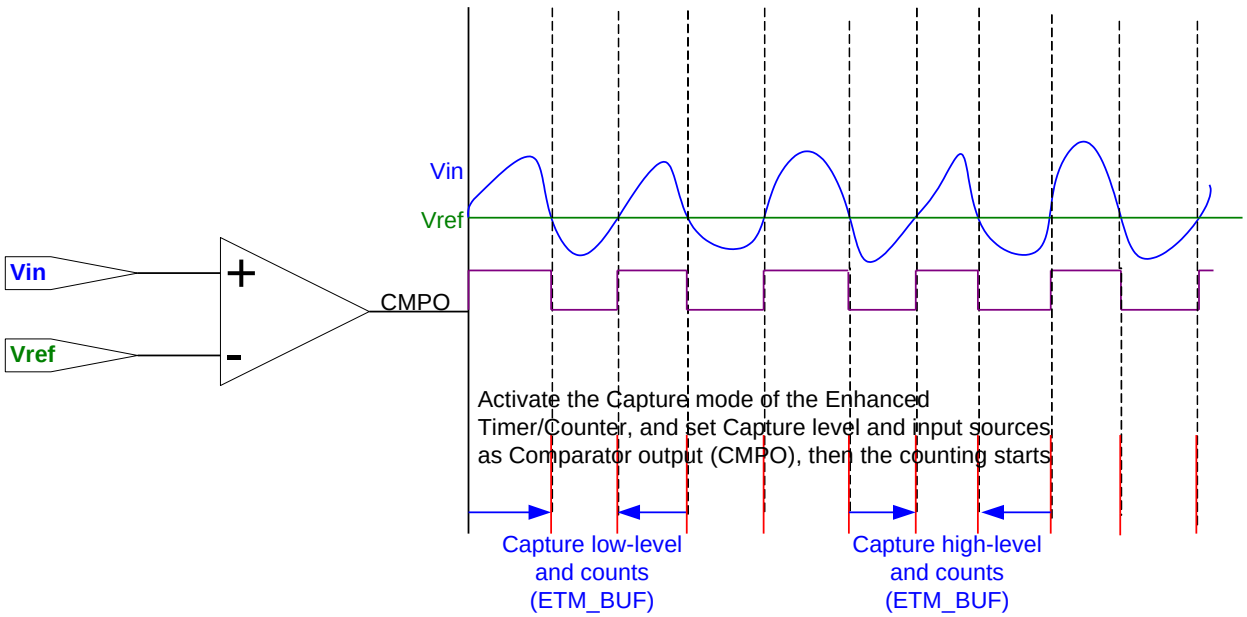
-: unimplemented.

Comparator Reference Voltage Table:

ACOMP_VREF[4:0]	CMPN Voltage (VDD = 3.3V; VSS = 0V)	$V_{Bandgap}$ = 1.262V
0	0.00	0.00
1	0.10	0.04
2	0.21	0.08
3	0.31	0.12
4	0.41	0.16
5	0.52	0.20
6	0.62	0.24
7	0.72	0.28
8	0.83	0.32
9	0.93	0.35
10	1.03	0.39
11	1.13	0.43
12	1.24	0.47
13	1.34	0.51
14	1.44	0.55

ACOMP_VREF[4:0]	CMPN Voltage (VDD = 3.3V; VSS = 0V)	$V_{Bandgap}$ = 1.262V
15	1.55	0.59
16	1.65	0.63
17	1.75	0.67
18	1.86	0.71
19	1.96	0.75
20	2.06	0.79
21	2.17	0.83
22	2.27	0.87
23	2.37	0.91
24	2.48	0.95
25	2.58	0.99
26	2.68	1.03
27	2.78	1.06
28	2.89	1.10
29	2.99	1.14
30	3.09	1.18
31	3.20	1.22

Example: The figure below shows comparator input via the enhanced timer to perform Gating Timer to capture low-level or high-level period.



6.16 Low Voltage Detection (LVD)

WT56F248/232 has a built-in Low Voltage Detection circuitry which can detect the supply voltage falls below the minimum specified operating voltage then generates an Interrupt.

- The Enable and Disable function of Low Voltage Detection are controlled by the software
- Low Voltage Detection level provides 8-level of voltage for selection: 2.00V, 2.25V, 2.50V, 2.75V, 3.00V, 3.25V, 3.50V or 3.75V

Low Voltage Detection Control Register LVD_CTL (XFR: 0x02) **Reset Value: A6h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	**R/W**	**R**	**R/W**	**R/W**	**R/W**	R/W	R/W	R/W
Name	**LVD_PD**	**LVD_CMP**	**LVD_LVL[2:0]**			LVD_RST_PD	LCD_RST_LVL[1:0]	

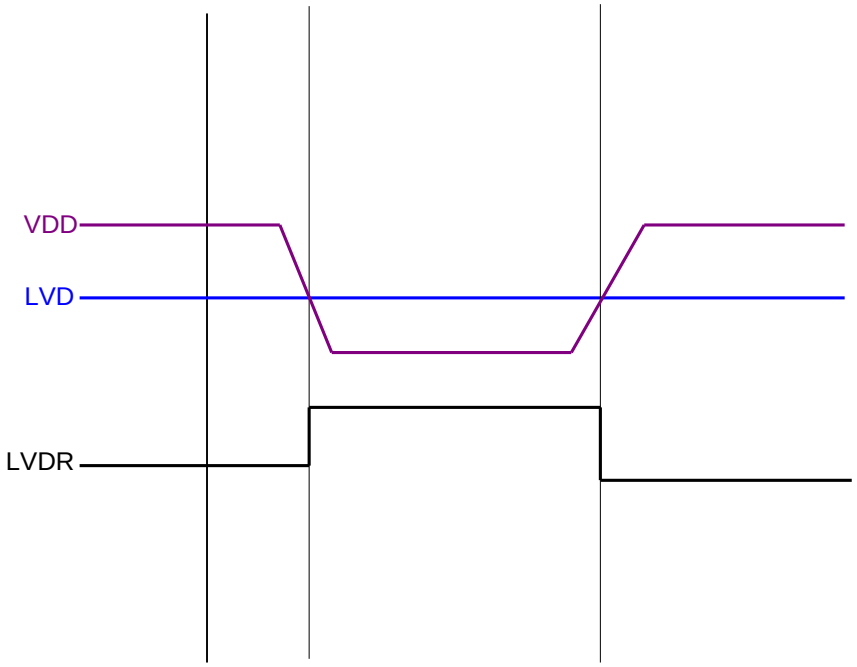
Bit Number	Bit Mnemonic	Description
7	LVD_PD	1: Power down Low Voltage Detection 0: Turn on Low Voltage Detection
6	LVD_CMP	Low Voltage Detection Compared Result 1: Power Voltage < setting Low Voltage Detection voltage 0: Power Voltage > setting Low Voltage Detection voltage
5-3	LVD_LVL[2:0]	Low Voltage Detection Range: 111: 3.75V 110: 3.50V 101: 3.25V 100: 3.00V 011: 2.75V 010: 2.50V 001: 2.25V 000: 2.00V

Note: The voltage range of Low Voltage Detection has great tolerance. Please refer to section 7.8 Electrical Characteristics for more details.

6.17 Low Voltage Detection Reset (LVDR)

WT56F248/232 has a built-in Low Voltage Detection circuitry which can detect the supply voltage falls below the minimum specified operating voltage then generates a Reset.

- The Enable and Disable function of Low Voltage Detection Reset are controlled by the software
- Low Voltage Detection level provides 4-level of voltage for selection: 2.00V, 2.50V, 3.00V or 3.50V



Low Voltage Detection Control Register LVD_CTL(XFR: 0x02) **Reset Value: A6h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R	R/W	R/W	R/W	**R/W**	**R/W**	**R/W**
Name	LVD_PD	LVD_CMP	LVD_LVL[2:0]			**LVD_RST_PD**	**LCD_RST_LVL[1:0]**	

Bit Number	Bit Mnemonic	Description
2	LVD_RST_PD	1: Turn off Low Voltage Detection Reset power 0: Turn on Low Voltage Detection Reset power
1-0	LVD_RST_LVL[1:0]	Low Voltage Detection Reset Range: 11: 3.50V 10: 3.00V 01: 2.50V 00: 2.00V

Note: The voltage range of Low Voltage Detection Reset has great tolerance. Please refer to section 7.8 Electrical Characteristics for more details.

Reset Flag Register RESET_FLG (XFR: 0x03) **Reset Value: 01h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	-	R	R	R	R	R	R
Name	CLR_RST_FLG	Reserved	ISP_RST_FLG	WDT_RST_FLG	NRST_FLG	LVD_RST_FLG	LVR_RST_FLG	POR_RST_FLG

Bit Number	Bit Mnemonic	Description
7	CLR_RST_FLG	1: Clear all Reset Flag
6	Reserved	-
5	ISP_RST_FLG	1: Reset source is from ISP
4	WDT_RST_FLG	1: Reset source is from Watchdog
3	NRST_FLG	1: Reset source is from External Reset pin
2	LVD_RST_FLG	1: Reset source is from Low Voltage Detection Reset
1	LVR_RST_FLG	1: Reset source is from Low Voltage Reset
0	POR_RST_FLG	1: Reset source is from External Power Reset

Note: For more details, refer to section 5.7 Reset.

6.18 Emulated E²PROM

The WT56F248/232 can use Flash PROM space to emulate E²PROM.
WT56F248 storage address locates from 0xB000 ~ 0xBEFF (3840 Bytes)
WT56F232 storage address locates from 0x7000 ~ 0x7EFF (3840 Bytes)

E²PROM Enable Register 1 EER_EN1[3:0] (XFR: 0xE0) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	W	W	W	W
Name	Reserved				EER_EN1[3:0]			

Bit Number	Bit Mnemonic	Description
7-4	Reserved	-
3-0	EER_EN1[3:0]	When EER_EN1[3:0] = '1010' and EER_EN2[3:0] = '0101', the E²PROM function is enabled.

-: unimplemented.

E²PROM Enable Register 2 EER_EN2[3:0] (XFR: 0xE1) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	W	W	W	W
Name	Reserved				EER_EN2[3:0]			

Bit Number	Bit Mnemonic	Description
7-4	Reserved	-
3-0	EER_EN2[3:0]	When EER_EN2[3:0] = '0101' and EER_EN1[3:0] = '1010', the E²PROM function is enabled.

-: unimplemented.

E²PROM Address Low Bytes Register EER_ADDR[7:0] (XFR: 0xE2) **Reset Value: FFh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	EER_ADDR[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	EER_ADDR[7:0]	EER_ADDR[7:0] address setting, paired with EER_ADDR[11:8] to form a 12-bit address

E²PROM Address High Bytes Register EER_ADDR[11:8] (XFR: 0xE3) **Reset Value: 0Fh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				EER_ADDR[11:8]			

Bit Number	Bit Mnemonic	Description
7-4	Reserved	-
3-0	EER_ADDR[11:8]	EEP_ADDR[11:8] address setting, paired with EER_ADDR[7:0] to form a 12-bit address

-: unimplemented.

E²PROM Control Register EER_TCTL[3:0] (XFR: 0xE4) **Reset Value: 08h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	W	W	W	W	W	W	W
Name	Reserved	ERR_IFREN	EER_ERASE	EER_PROG	EER_TCTL[3:0]			

Bit Number	Bit Mnemonic	Description
7	Reserved	-
6	ERR_IFREN	Must be set as “0”
5	EER_ERASE	1: E²PROM proceeds ERASE **(512 Bytes)** /page 0: Did not proceed ERASE
4	EER_PROG	1: E²PROM proceeds PROGRAM (1 Byte) 0: Did not proceed PROGRAM
3-0	EER_TCTL[3:0]	E²PROM ERASE/PROGRAM time setting (see Note)

-: unimplemented.

E²PROM Data Register EER_DATA[7:0] (XFR: 0xE8) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	EER_DATA[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	EER_DATA[7:0]	E²PROM Data Register

Notes 1: MCU clock will be turned off in programming or erasing E²PROM, and thus all functions of 8052 are halt state. Please refer to 3.1 System Clock Tree for more details.

Notes 2: Recommended:
Only if MCU_CLK = 12 MHz, programming or erasing E²PROM is allowed, and EER_TCTL[3:0] can be set as “1000”. Thus, the programming time of 1 Byte = 24u sec ~ 32u sec. The erasing time of 1 Bank (512 Bytes) = 32m sec ~ 36m sec.

Notes 3: LVR must be disabled prior to programming or erasing E²PROM; LVR can be enabled only after programming or erasing E²PROM is finished. Please refer to E²PROM Enable Flow Chart for more details.

WT56F248 E^{2}PROM Clear Range and Address Setting (Cleared data 0xFF)

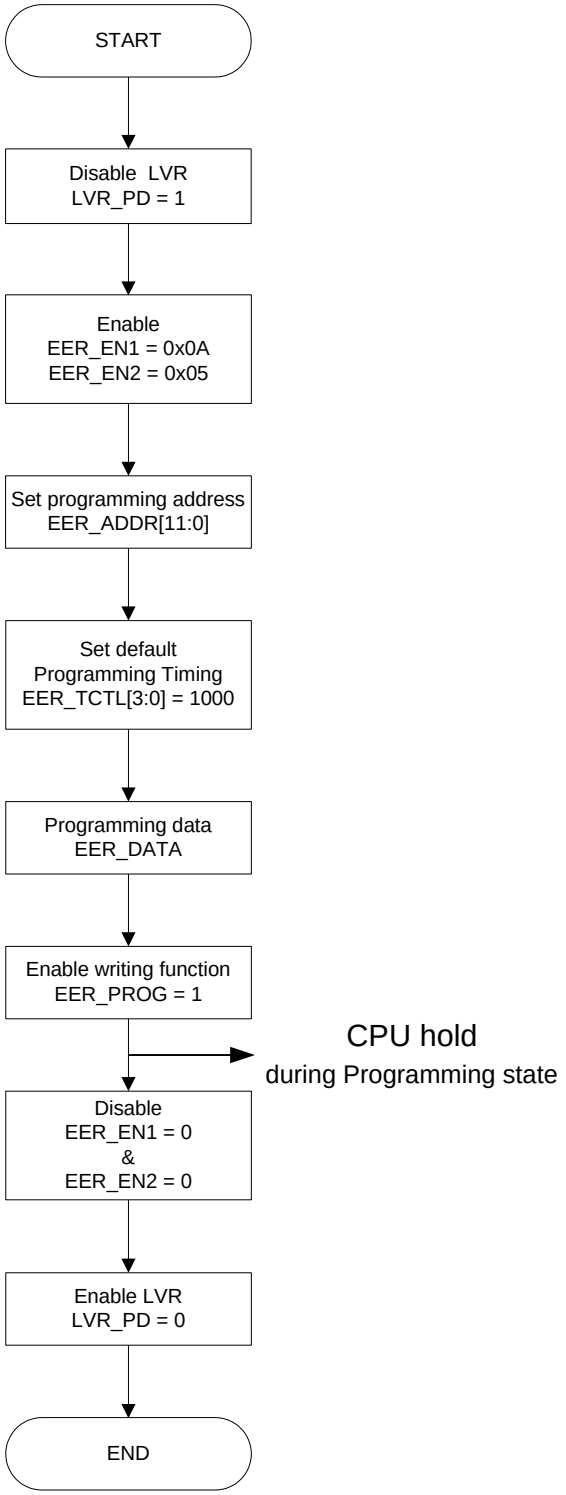
Flash address	EER_ADDR[11:8]	EER_ADDR[7:0]	Erase Range	Remark
0xB000	0000	0000 0000	0xB000 ~ 0xB1FF	
0xB200	0010	0000 0000	0xB200 ~ 0xB3FF	
0xB400	0100	0000 0000	0xB400 ~ 0xB5FF	
0xB600	0110	0000 0000	0xB600 ~ 0xB7FF	
0xB800	1000	0000 0000	0xB800 ~ 0xB9FF	
0xBA00	1010	0000 0000	0xBA00 ~ 0xBBFF	
0xBC00	1100	0000 0000	0xBC00 ~ 0xBDFF	

WT56F232 E²PROM Clear Range and Address Setting (Cleared data 0xFF)

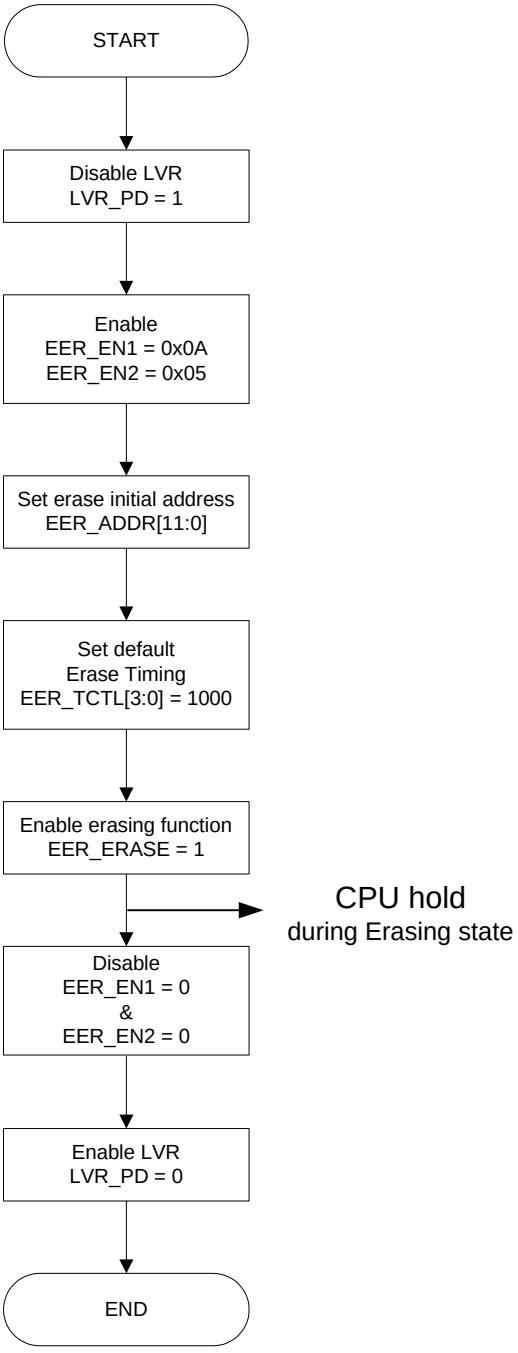
Flash address	EER_ADDR[11:8]	EER_ADDR[7:0]	Erase Range	Remark
0x7000	0000	0000 0000	0x7000 ~ 0x71FF	
0x7200	0010	0000 0000	0x7200 ~ 0x73FF	
0x7400	0100	0000 0000	0x7400 ~ 0x75FF	
0x7600	0110	0000 0000	0x7600 ~ 0x77FF	
0x7800	1000	0000 0000	0x7800 ~ 0x79FF	
0x7A00	1010	0000 0000	0x7A00 ~ 0x7BFF	
0x7C00	1100	0000 0000	0x7C00 ~ 0x7DFF	

E²PROM Enable Flow chart:

Programming function:



Erasing function:



6.19 Code Option

Code Block located in the last eight bytes of Flash ROM for storing customer ID and IC configuration with address listed as the following table.

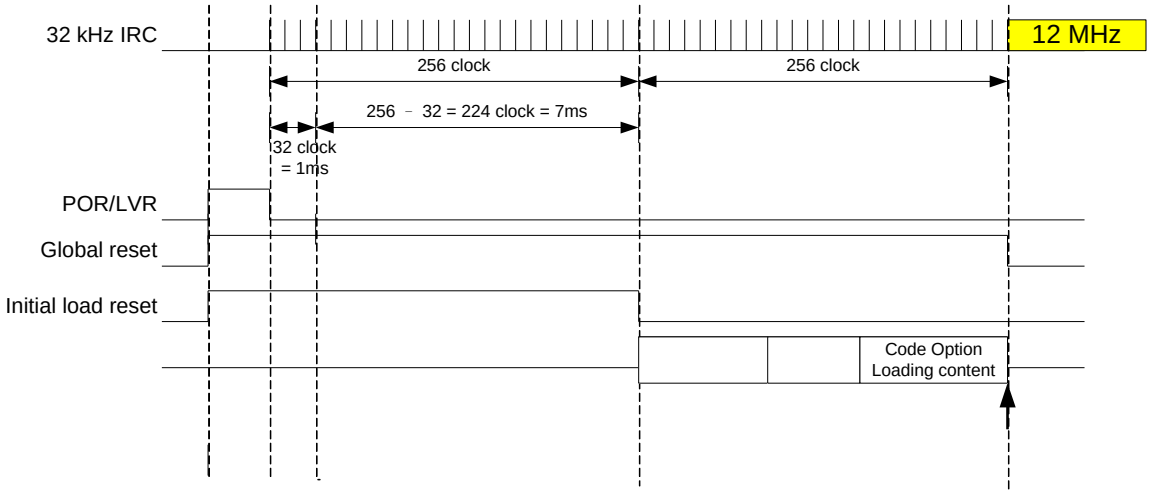
If this function is not enabled, please reserve the space of these eight bytes, and fill it with 0xFF.

If the function is enabled, WT56F248/232 will auto reload the code option at each reset. Please refer to the Sequency Diagram as listed below.

Address	Bit Number	Description
BFF8H / 7FF8H	**7-0**	**= AFH, enable Code Option function. If the higher 4 bits of this byte is "1010", Code Option is enabled.** **= FFH, disable Code Option function** **Default value 0xFF**
BFF9H / 7FF9H	7-0	Customer ID 1, mapping to XFR: CSM_ID1 0x0D[7:0] Default value 0xFF: code can be assigned by SWUT ISP software programming
BFFAH / 7FFAH	7-0	Customer ID 2, mapping to XFR: CSM_ID2 0x0E[7:0] Default value 0xFF: code can be assigned by SWUT ISP software programming
BFFBH / 7FFBH	7-0	Customer ID 3, mapping to XFR: CSM_ID3 0x0F[7:0] Default value 0xFF: code can be assigned by SWUT ISP software programming
BFFCH / 7FFCH	7-0	Flash memory content protection: **it is an individual setting, and will not be turned off even if Code Option is disabled.** = 10H flash memory cannot be read = 00H flash memory cannot be written into Default value 0xFF: Flash can read/write (by code encryption to achieve the same protection)
General Purpose I/O Complex Function Options Setting:		
BFFDH / 7FFDH	7-6	Reserved
	5	Mapping to XFR: GPA5_FUN_SLT 0x25H[3] 1: Sub crystal 0: GPIO (default)
	4	Mapping to XFR: GPA2_FUN_SLT 0x26H[5] 1: Main crystal 0: GPIO (default)
	3	Mapping to XFR: GPF3_FUN_SLT 0x2FH[7] 1: NRST 0: GPIO (default)
	2	Mapping to XFR: LVD_RST_PD 0x02H[2] 1: disable Low Voltage Reset (default) 0: enable Low Voltage Reset
	1-0	Mapping to XFR: LVD_RST_LVL 0x02H[1:0], Low Voltage Detection and Reset level setting 00: 2.00V 01: 2.50V 10: 3.00V (default) 11: 3.50V

Oscillator Initialization and Driving Ability Options Setting:		
BFFEH / 7FFEH	7-5	Reserved
	4-3	Mapping to XFR: SOURCE_CLK_SLT[1:0] 0x05H[3:2]; initialization value of main oscillator 00: SOURCE clock = internal 12 MHz RC oscillator (default) 01: SOURCE clock = external 1 MHz ~ 24 MHz crystal oscillator 10: SOURCE clock = internal 32 kHz RC oscillator 11: SOURCE clock = external 32.768 kHz crystal oscillator
	2-1	Mapping to XFR: CRY_12M_DR[1:0] 0x08H[2:1]; oscillator driving ability selection 00: select < 100 kHz crystal oscillator 01: select 100 kHz ~ 1 MHz crystal oscillator 10: select 1 MHz ~ 12 MHz crystal oscillator (default) 11: select 12 MHz ~ 24 MHz crystal oscillator
	0	Mapping to XFR: BLDO_PD 0x08H[0]; internal voltage regulator (main LDO) 1: turn off 0: turn on (default)
All Oscillator Power Switch Options Setting:		
BFFFH / 7FFFH	7-5	Reserved
	4	Mapping to XFR: IRC_12M_PD1 0x07H[4] 1: turn off partial power of internal 12 MHz RC oscillator 0: turn on partial power of internal 12 MHz RC oscillator (default)
	3	Mapping to XFR: IRC_12M_PD2 0x07H[3] 1: turn off all power of internal 12 MHz RC oscillator 0: turn on all power of internal 12 MHz RC oscillator (default)
	2	Mapping to XFR: IRC_32K_PD 0x07H[2] 1: turn off the power of internal 32 kHz RC oscillator 0: turn on the power of internal 32 kHz RC oscillator (default)
	1	Mapping to XFR: CRY_12M_PD 0x07H[1] 1: Turn off external 1 MHz ~ 24 MHz crystal oscillator (default) 0: Turn on external 1 MHz ~ 24 MHz crystal oscillator
	0	Mapping to XFR: CRY_32K_PD 0x07H[0] 1: Turn off external 32.768 kHz crystal oscillator (default) 0: Turn on external 32.768 kHz crystal oscillator

Note: Code option setting would be overwritten by program setting, it is recommended to use the program to set the code option. Please refer to the next page for code option setting examples and code example program.



Switched by IRC 32 kHz
IRC 12 MHz or CRY 12 MHz

```
WT56F248/232 Code Option example:
; This Code : CodeOption248.A51 is for WT56F248/232 Code Option Setting
;--------------------------------------------------------------------------------
#define OPTION_ON              1
#define OPTION_OFF             0
;; Default Code Option OFF
#define WT56F248/232_CODE_OPTION     OPTION_OFF


    #if(WT56F248/232_CODE_OPTION==OPTION_ON)
    ;;Load Code option switch
    CSEG       AT 0xBFF8 / 7FF8H
    DB         10101111B  ;;0xAF: load code option

    ;;Customer ID 1 default 0xFF
    CSEG       AT 0xBFF9 / 7FF9H
    DB         11111111B
    ;;Customer ID 2 default 0xFF
      CSEG       AT 0xBFFA / 7FFAH
    DB         11111111B
    ;;Customer ID 3 default 0xFF
      CSEG       AT 0xBFFB / 7FFBH
    DB         11111111B
    ;;Flash Protect Read/Write
      CSEG       AT 0xBFFC / 7FFCH
    ;;Flash memory content protection:
    ;;default 0xFF select no protection MCU can read/write
    ;;bit7-0 = 10H flash memory cannot be read
    ;;bit7-0 = 00H flash memory cannot be written into
    DB         11111111B

    ;;Crystal GPIO setting
      CSEG       AT 0xBFFD / 7FFDH
    ;;bit7 NC     default 0
    ;;bit6 NC     default 0
    ;;bit5 Mapping to XFR: GPA5_FUN_SLT 0x25H[3]
        ;;default 0
        ;;1: Sub crystal
        ;;0: GPIO
    ;;bit4 Mapping to XFR: GPA2_FUN_SLT 0x26H[5]
        ;;default 0
        ;;1: Main crystal
        ;;0: GPIO
    ;;bit3 Mapping to XFR: GPF3_FUN_SLT 0x2FH[7]
        ;;default 0 select GPIO
        ;;1: NRST
        ;;0: GPIO
    ;;bit2 Mapping to XFR: LVD_RST_PD 0x02H[2]
        ;;default 1 select disable
        ;;1: disable low voltage reset
        ;;0: enable low voltage reset
    ;;bit1-0   Mapping to XFR: LVD_RST_LVL 0x02H[1:0], low voltage detection and reset level setting
        ;;default 10 select 3.00V
        ;;00: 2.00V
        ;;01: 2.50V
        ;;10: 3.00V
```

```
    ;;11: 3.50V
DB      00000110B

;;Source Clock and Crystal drive setting
  CSEG    AT 0xBFFE / 7FFEH
;;bit7 NC    default 0
;;bit6 NC    default 0
;;bit5 NC    default 0
;;bit4-3  Mapping to XFR: SOURCE_CLK_SLT[1:0] 0x05H[3:2]; initialization value of main oscillator
    ;;default 00
    ;;00: SOURCE clock = internal 12 MHz RC oscillator
    ;;01: SOURCE clock = external 1 MHz ~ 24 MHz crystal oscillator
    ;;10: SOURCE clock = internal 32 kHz RC oscillator
    ;;11: SOURCE clock = external 32.768 kHz crystal oscillator
;;bit2-1  Mapping to XFR: CRY_12M_DR[1:0] 0x08H[2:1]; oscillator driving ability selection
    ;;default 10
    ;;00: select < 100 kHz crystal oscillator
    ;;01: select 100 kHz ~ 1 MHz crystal oscillator
    ;;10: select 1 MHz ~ 12 MHz crystal oscillator
    ;;11: select 12 MHz ~ 24 MHz crystal oscillator
;;bit0 Mapping to XFR: BLDO_PD 0x08H[0]; internal voltage regulator (main LDO)
    ;;default turn on
    ;;1: turn off
    ;;0: turn on
DB      00000100B

;;Crystal Power setting
  CSEG    AT 0xBFFF / 7FFFH
;;bit7 NC    default 0
;;bit6 NC    default 0
;;bit5 NC    default 0
;;bit4 Mapping to XFR: IRC_12M_PD1 0x07H[4] default turn on
    ;;1: turn off partial power of internal 12 MHz RC oscillator
    ;;0: turn on partial power of internal 12 MHz RC oscillator
;;bit3 Mapping to XFR: IRC_12M_PD2 0x07H[3] default turn on
    ;;1: turn off all power of internal 12 MHz RC oscillator
    ;;0: turn on all power of internal 12 MHz RC oscillator
;;bit2 Mapping to XFR: IRC_32K_PD 0x07H[2] default turn on
    ;;1: turn off the power of internal 32 kHz RC oscillator
    ;;0: turn of the power of internal 32 kHz RC oscillator
;;bit1 Mapping to XFR: CRY_12M_PD 0x07H[1] default turn off
    ;;1: Turn off external 1 MHz ~ 24 MHz crystal oscillator
    ;;0: Turn on external 1 MHz ~ 24 MHz crystal oscillator
;;bit0 Mapping to XFR: CRY_32K_PD 0x07H[0] default turn off
    ;;1: Turn off external 32.768 kHz crystal oscillator
    ;;0: Turn on external 32.768 kHz crystal oscillator
DB      00000011B
#else
CSEG    AT 0xBFF8 / 7FF8H
DB      11111111B
CSEG    AT 0xBFF9 / 7FF9H
DB      11111111B
CSEG    AT 0xBFFA / 7FFAH
DB      11111111B
CSEG    AT 0xBFFB / 7FFBH
DB      11111111B
```

```
CSEG    AT 0xBFFC / 7FFCH
DB      11111111B
CSEG    AT 0xBFFD / 7FFDH
DB      11111111B
CSEG    AT 0xBFFE / 7FFEH
DB      11111111B
CSEG    AT 0xBFFF / 7FFFH
DB      11111111B
#endif
```

Customer ID 1 ~ 3 mapped to the Customer Code Registers, please refer to the following customer code register.

Customer Code Register 1 CSTM_ID1 (XFR: 0x0D) **Reset Value: FFh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CSTM_ID1							

Bit Number	Bit Mnemonic	Description
7-0	CSTM_ID1	Customer code, paired with CSTM_ID2 and CSTM_ID3, 3 bytes in total.

Customer Code Register 2 CSTM_ID2 (XFR: 0x0E) **Reset Value: FFh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CSTM_ID2							

Bit Number	Bit Mnemonic	Description
7-0	CSTM_ID2	Customer code, paired with CSTM_ID3 and CSTM_ID1, 3 bytes in total.

Customer Code Register 3 CSTM_ID3 (XFR: 0x0F) **Reset Value: FFh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CSTM_ID3							

Bit Number	Bit Mnemonic	Description
7-0	CSTM_ID3	Customer code, paired with CSTM_ID1 and CSTM_ID2, 3 bytes in total.

Note: WT56F248/232 provides three bytes (24 bits) of code option, which can be set by customer to read data from program storage after reset.

The following registers are described in the previous section, and now are set for the Code Option registers mapped in the General-purpose I/O Complex Function options, including the Option settings of the crystal oscillator pins, Reset, and Low Voltage Detection Reset.
0x25, 0x26, 0x2F, 0x02 registers again described as below.

General-purpose I/O Port A Complex Function Setting Register1 GPIOA_FUN1 (XFR: 0x25) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	-	-	-
Name	GPA7_FUN_SLT[1:0]		GPA6_FUN_SLT[1:0]		GPA5_FUN_SLT	Reserved		

Bit Number	Bit Mnemonic	Description
7-6	GPA7_FUN_SLT[1:0]	Set GPIOA7D complex function 00: GPIO/IRQ7 (default) 01: PWM1 output of Path A 10: ETMO output 11: ADC0 input
5-4	GPA6_FUN_SLT[1:0]	Set GPIOA6D complex function 00: GPIO/IRQ6 (default) 01: PWM2 output of Path A 10: SPI STBB input pin 11: -
3	GPA5_FUN_SLT	Set GPIOA5D complex function 1: XSOUT (served as sub crystal oscillator output pin, and was forced to set GPIOA4D as sub crystal oscillator input pin (XSIN) instead of GPIO function) 0: GPIO (default), and meanwhile GPIOA4 will be set as GPIO function.
2-0	Reserved	-

-: unimplemented.

Notes: The setting of using External Sub Crystal Oscillator as SOURCE clock:

1. Set GPIOA5 and GPIOA4 as Input port. (XFR 0x10 GPIOA_OE[5:4])
2. GPIOA5 and GPIOA4 disable internal pull high resistor. If enable pull high resistor will result in oscillator outputs unstable frequency. (XFR 0x1C GPIOA_PHN[5:4])
3. Set GPIOA5 and GPIOA4 as Sub Crystal Oscillator pin. (XFR 0x25 GPA5_FUN_SLT)
4. Set the driving ability of External Sub Crystal Oscillator. (XFR 0x01 SPEEDUP_C32K[1:0])
5. Power on External Crystal Oscillator switch. (XFR 0x07 CRY_32K_PD)
6. Switch SOURCE clock to External Crystal Oscillator. (XFR 0x05 SOURCE_CLK_SLT[1:0])

General-purpose I/O Port A Complex Function Setting Register2 GPIOA_FUN2 (XFR: 0x26) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	-	-	-	R/W	-
Name	GPA3_FUN_SLT[1:0]		GPA2_FUN_SLT	Reserved			GPA0_FUN_SLT	Reserved

Bit Number	Bit Mnemonic	Description
7-6	GPA3_FUN_SLT[1:0]	Set GPIOA3D complex function 00: GPIO/IRQ5 (default) 01: I²C SDA data pin, and was forced to set GPIOE7DH as I²C SCL pin instead of GPIO function 10: SPI MISO data pin 11: P03 output/input (mapping to 8052 P0.3) PWM3 output of Path A Regarding the pin setting, please refer to GPA3_FUN_SLT2 (Address 0x0221)
5	GPA2_FUN_SLT	Set GPIOA2D complex function 1: XMIN (main crystal oscillator input pin), will auto define GPIOA1D as main crystal oscillator output pin without GPIO function 0: GPIO (default)
4-2	Reserved	-
1	GPA0_FUN_SLT	Set GPIOA0D complex function 1: SPI MOSIB data pin 0: GPIO/IRQ4 (default)
0	Reserved	-

-: unimplemented.

Notes: The setting of using External Main Crystal Oscillator as SOURCE clock:

1. Set GPIOA2 and GPIOA1 as Input port. (XFR 0x10 GPIOA_OE[2:1])

2. GPIOA2 and GPIOA1 disable internal pull high resistor. If enable pull high resistor will result in oscillator outputs unstable frequency. (XFR 0x1C GPIOA_PHN[2:1])

3. Set GPIOA2 and GPIOA1 as Main Crystal Oscillator pin. (XFR 0x26 GPA2_FUN_SLT)

4. Set the driving ability of External Main Crystal Oscillator. (XFR 0x08 CRY_12M_DR[1:0])

5. Power on External Crystal Oscillator. (XFR 0x07 CRY_12M_PD)

6. Switch SOURCE clock to External Crystal Oscillator. (XFR 0x05 SOURCE_CLK_SLT[1:0])

General-purpose I/O Port F Complex Function Setting Register GPF_FUN (XFR: 0x2F) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPF3_FUN_SLT	Reserved	GPF2_FUN_SLT[1:0]		GPF1_FUN_SLT[1:0]		GPF0_FUN_SLT[1:0]	

Bit Number	Bit Mnemonic	Description
7	GPF3_FUN_SLT	Set GPIF3 function 1: Reset pin (NRST) input 0: GPIO (default)
6	Reserved	-
5-4	GPF2_FUN_SLT[1:0]	Set GPIOF2DH function 00: GPIO/IRQ3 (default)

Bit Number	Bit Mnemonic	Description
		01: CMPO, comparator output 10: T2CAP/SPI STBA (Input) 11: P02 output/input PWM3 output of Path B Regarding the pin setting, please refer to GPF2_FUN_SLT2 (Address 0x022B)
3-2	GPF1_FUN_SLT[1:0]	Set GPIOF1DH function 00: GPIO/CMPN/IRQ2 (default) 01: T2 input, Timer/counter2 external clock source input 10: SPI MOSIA data pin 11: P01 output/input (mapping to 8052 P0.1) **Note: When GPIOF1 selects CMPN function, it must be set as GPIO Input.** PWM2 output of Path B Regarding the pin setting, please refer to GPF1_FUN_SLT2 (Address 0x022B)
1-0	GPF0_FUN_SLT[1:0]	Set GPIOF0DH function 00: GPIO/CMPP/IRQ1 (default) 01: PWM0A, PWM0 output of Path A 10: T2O output, Timer/counter2 overflow output 11: BUZOA, Buzzer output **Note: When GPIOF0 selects CMPP function, it must be set as GPIO Input.**

-: unimplemented.

Low Voltage Detection Control Register LVD_CTL(XFR: 0x02) Reset Value: A6h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	**R/W**	**R**	**R/W**	**R/W**	**R/W**	R/W	R/W	R/W
Name	**LVD_PD**	**LVD_CMP**	**LVD_LVL[2:0]**			LVD_RST_PD	LCD_RST_LVL[1:0]	

Bit Number	Bit Mnemonic	Description
7	LVD_PD	1: Power down Low Voltage Detection 0: Turn on Low Voltage Detection
6	LVD_CMP	Low Voltage Detection Compared Result 1: Power Voltage < setting Low Voltage Detection voltage 0: Power Voltage > setting Low Voltage Detection voltage
5-3	LVD_LVL[2:0]	Low Voltage Detection range: 111: 3.75V 110: 3.50V 101: 3.25V 100: 3.00V 011: 2.75V 010: 2.50V 001: 2.25V 000: 2.00V

The following section illustrates the Code Option setting initialization oscillator & driving ability option setting mapped registers, which contains the option setting of crystal oscillator source and driving ability.

System Clock Source Control Register SOURCE_CLK_SLT (XFR: 0x05) **Reset Value: A0h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				SOURCE_CLK_SLT[1:0]		MCU_CLK_SLT[1:0]	

Bit Number	Bit Mnemonic	Description
7-4	-	Must be equal to “1010”, otherwise bit [3:0] cannot be written into.
3-2	SOURCE_CLK_SLT[1:0]	Select SOURCE clock sources 00: internal 12 MHz RC oscillator (default) 01: external DC ~ 24 MHz crystal oscillator 10: internal 32 kHz RC oscillator 11: external 32.768 kHz crystal oscillator Default value can be selected by section 6.19 Code Option Select
1-0	MCU_CLK_SLT[1:0]	MCU clock setting 00: MCU clock = SOURCE clock (default) 01: MCU clock = SOURCE clock /2 10: MCU clock = SOURCE clock /4 11: MCU clock = SOURCE clock /12

-: unimplemented.

Oscillator Driver Control Register CRY_12M_DR[1:0] (XFR: 0x08) **Reset Value: 54h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	R/W	R/W	R/W
Name	Reserved				Reserved	CRY_12M_DR[1:0]		BLDO_PD

Bit Number	Bit Mnemonic	Description
7-4	-	Must be equal to“0101”, otherwise, Bit[3:0] cannot be written into
3	Reserved	-
2-1	CRY_12M_DR[1:0]	External oscillator driving ability setting 00: crystal oscillator with frequency of 32768 Hz 01: crystal oscillator with frequency of 100 kHz ~ 1 MHz 10: crystal oscillator with frequency of 1 MHz ~ 12 MHz (default) 11: crystal oscillator with frequency of 12 MHz ~ 24 MHz Default value can be selected by section 6.19 Code Option Select
0	BLDO_PD	Internal voltage regulator (main LDO) 1: turn off main LDO 0: turn on main LDO (default) Default value can be selected by section 6.19 Code Option Select

-: unimplemented.

Note: Main LDO is turned off only on Green mode, if SOURCE clock is 12 MHz (IRC internal or external crystal oscillator) must be turned on, otherwise will result in failure and cannot program.

The following section illustrates the Code Option set all oscillator power switch option setting, and the setting according to the Reset Value is recommended. If use external crystal oscillator, please set the option while MCU executing procedures.

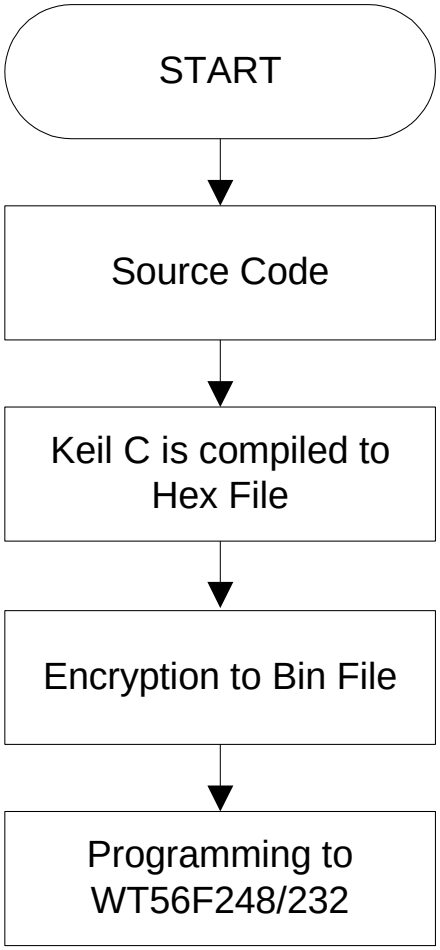
Clock Source Control Register IRC_12M_PD (XFR: 0x07) **Reset Value: A3h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	R/W	R/W	R/W	R/W	R/W
Name	Reserved			IRC_12M_PD1	IRC_12M_PD2	IRC_32K_PD	CRY_12M_PD	CRY_32K_PD

Bit Number	Bit Mnemonic	Description
7-5	-	Must be equal to “101”, otherwise bit[4:0] cannot be written into
4	IRC_12M_PD1	1: partial internal 12 MHz RC oscillator power is turned off (bias ON) (default value is not off) 0: not off
3	IRC_12M_PD2	1: all internal 12 MHz RC oscillator power are closed (bias off) (default value is not off) 0: not off
2	IRC_32K_PD	1: internal 32 kHz RC oscillator power is turned off (default value is not off) 0: not off
1	CRY_12M_PD	1: external 12 MHz crystal oscillator power is turned off (default value is off) 0: not off
0	CRY_32K_PD	1: external 32.768 kHz crystal oscillator power is turned off (default value if off) 0: not off

-: unimplemented.

6.20 Read Out Protection & Code Encryption



7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Range	Units
D.C. Supply Voltage	V_{DD}		-0.3 ~ 6.0	V
Input Voltage	V_I		-0.3 to V_{DD} +0.3	V
Output Voltage	V_O		-0.3 to V_{DD} +0.3	V
Total current source by all GPIO	$\sum I_{OH}$		90 @ -40℃ ~ +105℃	mA
Total current sink by all GPIO	$\sum I_{OL}$		90 @ -40℃ ~ +105℃	mA
Ambient Temperature	T_A		-40 ~ 125	℃
Storage Temperature	T_{STG}		-60 ~ 125	℃

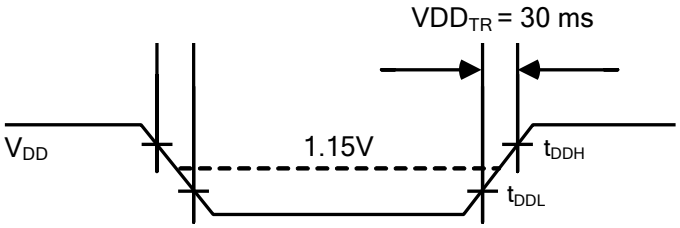
Note: Stresses above those listed may cause permanent damage to the devices.

7.2 Recommended Operating Parameters

Parameter	Symbol	Condition	Specification			Units
			Min	Typ.	Max	
Power Voltage	V_{DD}	F_{main} = 12 MHz	2.2		5.5	V
Main Frequency	F_{main}	V_{DD} = 2.2V ~ 5.5V		12		MHz
Sub Frequency	F_{sub}	V_{DD} = V_{DD}		32.768		kHz
Operating Temperature	T_{OPR}		-40		105	℃
POR (Power on Reset) Level	V_{POR}	At VDD_{TR} = 30ms, T_A = 25℃ (see table below)		1.15		V
VDD Rising Rate(*)	VDD_{TRA}		50			μS /V
VDD Falling Rate(*)	VDD_{TFA}		150			μS /V

(*): These parameters are presented for design guidance only and not tested or guaranteed.

Power On Reset (POR) Timing



7.3 DC Electrical Characteristics (V_{DD} = 2.2V ~ 5V, -40℃ ~ +105℃)

Parameter	Symbol	Condition	Specification			Units
			Min	Typ.	Max	
Schmitt Trigger from Low to High	V_{T+}	V_{DD} = 2.2V ~ 5.5V	0.6 V_{DD}		V_{DD} +0.3	V
Schmitt Trigger from High to Low	V_{T-}	V_{DD} = 2.2V ~ 5.5V			0.2 V_{DD}	V
Output High Voltage (Note)	V_{OH4}	I_{OH} = 4 mA at V_{DD} = 5V GPIOA0 ~ GPIOA7, GPIOB0 ~ GPIOB7, GPIOC0 ~ GPIOC7, GPIOD0 ~ GPIOD7	V_{DD} - 0.4			V
	V_{OH8}	I_{OH} = 8 mA at V_{DD} = 5V GOIOE0 ~ GPIOE7, GPIOF0 ~ GPIOF2	V_{DD} - 0.4			
Output Low Voltage (Note)	V_{OL4}	I_{OL} = 4 mA at V_{DD} = 5V GPIOA0 ~ GPIOA7, GPIOB0 ~ GPIOB7, GPIOC0 ~ GPIOC7, GPIOD0 ~ GPIOD7			V_{SS} +0.4	V
	V_{OL8}	I_{OL} = 8 mA at V_{DD} = 5V GOIOE0 ~ GPIOE7, GPIOF0 ~ GPIOF4			V_{SS} +0.4	
Input Leakage Current(*)	I_{OZ}	V_O = 0V or VDDV		±0.01	±1	μA
Pull-up Resistor	R_{PH}	V_{DD} = 5V, V_{PIN} = 0V		33		KΩ
Normal mode at 24 MHz Working Current	I_{VDD24M}	No load on output (V_{DD} = 5V, CRY24M on), peripheral off		6.5		mA
Normal mode at 12 MHz Working Current	I_{VDD12M}	No load on output (V_{DD} = 5V, CRY12M on), peripheral off		4.0		mA
		No load on output (V_{DD} = 5V, IRC12M on), peripheral off		3.5		mA
Normal mode at 6 MHz Working Current	I_{VDD6M}	No load on output (V_{DD} = 5V, IRC12M on), peripheral off		2.6		mA
Normal mode at 3 MHz Working Current	I_{VDD3M}	No load on output (V_{DD} = 5V, IRC12M on), peripheral off		1.5		mA
Normal mode at 1 MHz Working Current	I_{VDD1M}	No load on output (V_{DD} = 5V, IRC12M on), peripheral off		0.9		mA

Parameter	Symbol	Condition	Specification			Units
			Min	Typ.	Max	
Idle mode Working Current	I_{VDDS1}	No load on output (V_{DD} = 5V, mcuClk = stop, Peripheral clock = IRC12M, BLDO on), peripheral off		660		μA
Green mode Working Current	I_{VDDS2}	No load on output (V_{DD} = 5V, mcuClk = IRC32K, Peripheral clock = IRC32K, BLDO off), LVR off), peripheral off		20		μA
		No load on output (V_{DD} = 5V, mcuClk = CRYSTAL 32kHZ, Peripheral clock = CRYSTAL 32kHz, BLDO off, LVR off), peripheral off		40		μA
Sleep mode Working Current	I_{VDDS3}	No load on output (V_{DD} = 5V, mcuClk = stop, Peripheral clock = stop, BLDO off, LVR off), peripheral off		5		μA
LCD ON Working Current	I_{LCD1}	Normal mode at 5V		20		μA
		Normal mode at 3V		15		μA
	I_{LCD2}	Heavy mode at 5V		50		μA
		Heavy mode at 3V		32		μA
	I_{LCD3}	Buffer mode at 5V		52		μA
		Buffer mode at 3V		42		μA

(*): These parameters are presented for design guidance only and not tested or guaranteed.

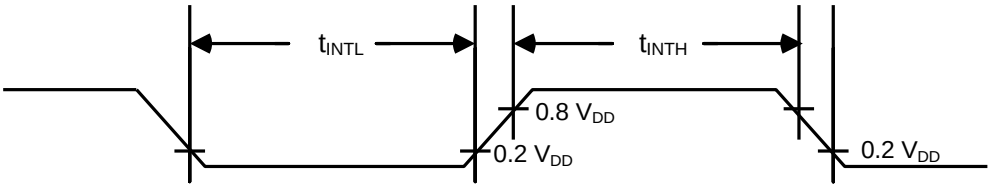
Note: V_{OH4} /V_{OL4} pins maximum sink/source current are 10mA; V_{OH8} /V_{OL8} pins maximum sink/source current are 20mA.

7.4 AC Electrical Characteristics (T_A = 25℃)

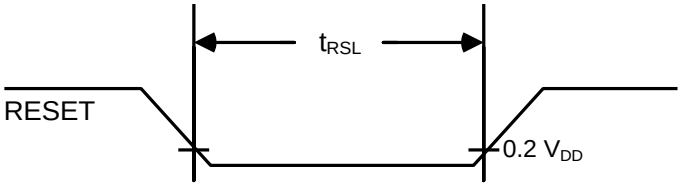
Parameter	Symbol	Pin/condition	Specification			Units
			Min	Typ.	Max	
Main Operation Frequency	F_{MCP}	X_{IN}	0.032		24	MHz
Sub Operation Frequency	F_{SCP}	SX_{IN}	32	32.768	35	kHz
Main Crystal Stabilization Time(*)		V_{DD} = 4.5V ~ 5.5V at 12 MHz			10	ms
		V_{DD} = 2.2V ~ 4.5V at 12 MHz			30	
		V_{DD} = 4.5V ~ 5.5V at 32768 Hz		0.5	1	s
		V_{DD} = 2.2V ~ 4.5V at 32768 Hz			10	s
Sub Crystal Stabilization Time(*) (32768 Hz only)		V_{DD} = 4.5V ~ 5.5V		0.5	1	s
		V_{DD} = 2.2V ~ 4.5V			10	s
Interrupt Input High, Low Width (IRQx)	t_{INTH}, t_{INTL}	MCU clock = 12 MHz	167			ns
RESET Input Low Width	t_{RSL}	RST_NDF = 1, main clock = 12 MHz	334			ns

(*): These parameters are presented for design guidance only and not tested or guaranteed.

Input Timing for External Interrupts



Input Timing for RESET



7.5 Internal 12/24 MHz RC Oscillator Temperature Tolerance table

Parameter	Symbol	Pin/condition	Specification			Units
			Min	Typ.	Max	
RC Oscillator Frequency	F_{RCH}	V_{DD} = 5V		12		MHz
Ex-factory Frequency Tolerance(*)	$\Delta F_{RCH1}/F_{RCH}$	Without external oscillator for calibrating 25℃		±1		%
		Without external oscillator for calibrating 0℃ ~ 70℃		±2		%
		Without external oscillator for calibrating -40℃ ~ 85℃		±3		%
		Without external oscillator for calibrating -40℃ ~ 125℃		±4		%
		With external oscillator for calibrating -40℃ ~ 125℃			±1	%

(*): These parameters are presented for design guidance only and not tested or guaranteed.

Parameter	Symbol	Pin/condition	Specification			Units
			Min	Typ.	Max	
RC Oscillator Frequency	F_{RCH}	V_{DD} = 5V		24		MHz
Ex-factory Frequency Tolerance(*)	$\Delta F_{RCH1}/F_{RCH}$	Without external oscillator for calibrating 25℃		±1		%
		Without external oscillator for calibrating 0℃ ~ 70℃		±2.5		%
		Without external oscillator for calibrating -40℃ ~ 85℃		±3.5		%
		Without external oscillator for calibrating -40℃ ~ 125℃		±5		%
		With external oscillator for calibrating -40℃ ~ 125℃			±1	%

(*): These parameters are presented for design guidance only and not tested or guaranteed.

7.6 A/D Converting Characteristics (T_A = 25℃)

Parameter	Symbol	Pin/condition	Specification			Units
			Min	Typ.	Max	
Resolution				12		bit
Integral Nonlinearity Error (INL)	E_{IL}	$AV_{REF} = V_{DD}$ = 5V		±4		LSB
Differential Nonlinearity Error (DNL)	E_{DL}	$AV_{REF} = V_{DD}$ = 5V		±2		LSB
Offset Error	E_{OFF}	$AV_{REF} = V_{DD}$ = 5V		±4		LSB
Gain Error	E_{GN}	$AV_{REF} = V_{DD}$ = 5V		±4		LSB
Operating Voltage At Vref = VDD/ExtVref	AV_{REF}	Absolute minimum to ensure 4 LSB accuracy	2.5		V_{DD}	V
Operating Voltage At Vref = BandGap 1.23V(*).		ADC_CLK = 125 kHz ensure 16 LSB accuracy	2.0			V
Operating Voltage At Vref = BandGap 2.44V(*)		ADC_CLK = 125 kHz ensure 8 LSB accuracy	2.7			V
Full-Scale Range	V_{ADCIN}		V_{SS}		V_{REF}	V
Recommended Impedance of Analog Voltage Source	Z_{AIN}				10	KΩ
Vref Input Current	I_{REF}	DAC base on different Vin	10		100	μA
		Comparator			200	μA
Conversion Time	T_{CT}	main clock = 12 MHz	16			ADC_clk
Ground Voltage(*)	AV_{SS}		V_{SS}		V_{SS} +0.3	V
ADC Working Current(*)	I_{ADC}	$AV_{REF} = V_{DD}$ = 5V		0.2		mA
		$AV_{REF} = V_{DD}$ = 5V at Power Down mode			1	μA

(*): These parameters are presented for design guidance only and not tested or guaranteed.

ADC ENOB (Effective number of bits)

Parameter	Pin/condition ADC convert time clock base = 500K	Specification			Units
		Min	Typ.	Max	
ENOB	AV_{REF} = V_{DD} = 5V ADC convert time clock base = 1 MHz		10		bit
	AV_{REF} = V_{DD} = 4V ADC convert time clock base = 1 MHz		10		bit
	AV_{REF} = V_{DD} = 3V ADC convert time clock base = 1 MHz		9.5		bit
	AV_{REF} = 2.44V (Bandgap) VDD > 2.7V ADC convert time clock base = 1.25 kHz		8		bit
	AV_{REF} = 1.23V (Bandgap) VDD > 2.2V ADC convert time clock base = 1.25 kHz		7		bit

7.7 Bandgap Electrical Characteristic

Parameter	Symbol	Pin/condition	Specification			Units
			Min	Typ.	Max	
Operating Voltage(*)		BGP = 1.23V	2.2		5.5	V
Operating Voltage(*)		BGP = 2.44V	2.7		5.5	V
Operating Temperature(*)			-40		105	℃
Bandgap Voltage	V_{BDIE}	V_{DD} = 5V Temp = 25℃		1.23 ±1% 2.44 ±1%		V
Voltage Variation	V_{BSP}	BGP = 1.23V		5		mV
		BGP = 2.44V		10		
Temperature Variation	V_{BTP}	Temp = -40℃~ 85℃ BGP = 1.22V		13		mV
		Temp = -40℃~ 85℃ BGP = 2.44V		25		mV

(*): These parameters are presented for design guidance only and not tested or guaranteed.

Note: Internal reference voltage Bandgap is calibrated out of factory at 2.44V±1% @VDD = 5V, please pay attention to the operating voltage.

7.8 Low Voltage Reset (LVR), Low Voltage Detection (LVD) & Low Voltage Detection Reset (LVDR) Electrical Characteristics (T_A = 25℃)

Parameter	Symbol	Pin/condition	Specification			Units
			Min	Typ.	Max	
LVR Voltage	V_{LVR}	$T_{A=}$ 25℃		1.5		V
LVR Working Current	I_{DDPR}	V_{DD} = 5V ±10%		5		μA
LVD & LVDR Response Time				120		μS
Low Voltage Detection Range Tolerance	V_{LVD}			±10		%
Low Voltage Detection Reset Range Tolerance	V_{LVDR}			±10		%

7.9 Comparator Characteristics (V_{DD} = 5V, T_A = 25℃)

Parameter	Symbol	Pin/condition	Specification			Units
			Min	Typ.	Max	
Comparator Input Voltage Range	V_{ICM}		V_{SS}		V_{DD}	V
Input Offset Voltage	V_{IOS}			±5		mV
Response Time	T_{RT}			1		μs
Setting Time(*)	T_{ST}	V_{DD} = 5 V		3	10	μs
32-level Reference Voltage Tolerance	V_{REF}			±10		%
Comparator Working Current	I_{CMP}	ACOMP_SEL_BGP [1:0] = 00		20		μA

(*): These parameters are presented for design guidance only and not tested or guaranteed.

7.10 LCD Characteristics (V_{DD} = 5V, T_A = 25℃)

Parameter	Symbol	Pin/condition	Specification			Units
			Min	Typ.	Max	
LCD Voltage Dividing Resister(*)	R_{LCD}	LCD_HLOAD = 1, LCD_BIAS = 10, 1/4 bias		60		kΩ
V_{LC4} Output Voltage	V_{LC4}	V_{DD} = 2.2V to 5.5V, 1/5 bias V_{LC5} = V_{DD}		0.8 V_{DD}		V
V_{LC3} Output Voltage	V_{LC3}			0.6 V_{DD}		V
V_{LC2} Output Voltage	V_{LC2}			0.4 V_{DD}		V
V_{LC1} Output Voltage	V_{LC1}			0.2 V_{DD}		V
Contrast Resolution(*)					5	Bits

(*): These parameters are presented for design guidance only and not tested or guaranteed.

7.11 Thermal Resistance Notice

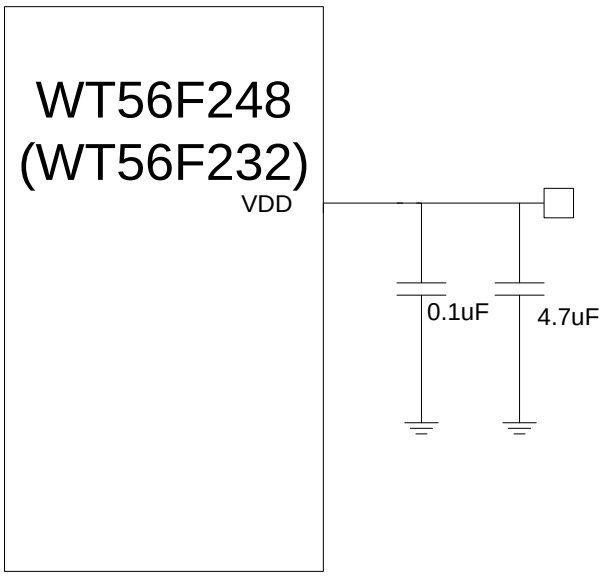
Parameter	Symbol	Feature	Value	Units	Condition
TH01	θJA	Thermal Resistance (Junction to Air)	57	℃/W	64-pin LQFP package
TH02	θJC	Thermal Resistance (Junction to Case)	15	℃/W	64-pin LQFP package
TH03	TJMAX	Maximum Junction Temperature	125	℃	64-pin LQFP package

Parameter	Symbol	Feature	Value	Units	Condition
TH01	θJA	Thermal Resistance (Junction to Air)	57	℃/W	44-pin LQFP package
TH02	θJC	Thermal Resistance (Junction to Case)	15	℃/W	44-pin LQFP package
TH03	TJMAX	Maximum Junction Temperature	125	℃	44-pin LQFP package

Parameter	Symbol	Feature	Value	Units	Condition
TH01	θJA	Thermal Resistance (Junction to Air)	34	℃/W	32-pin QFN package
TH02	θJC	Thermal Resistance (Junction to Case)	1.1	℃/W	32-pin QFN package
TH03	TJMAX	Maximum Junction Temperature	TBD	℃	32-pin QFN package

8. Application Circuits

8.1 Power Supply



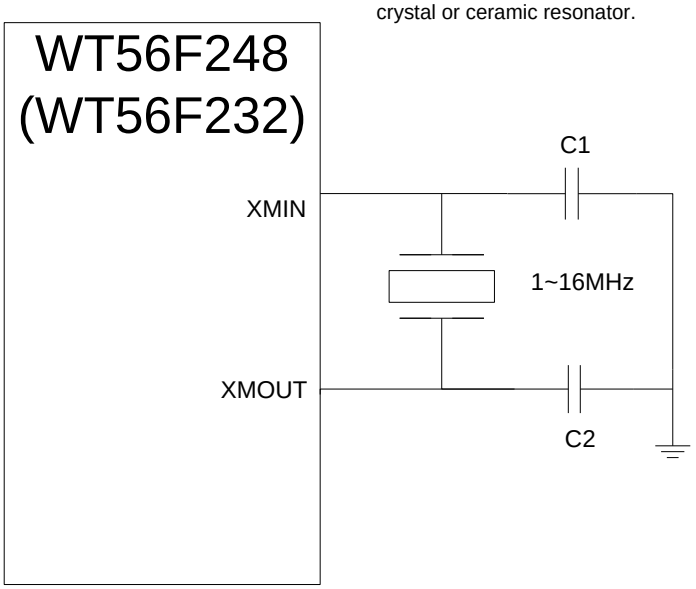
8.2 Oscillator Circuits

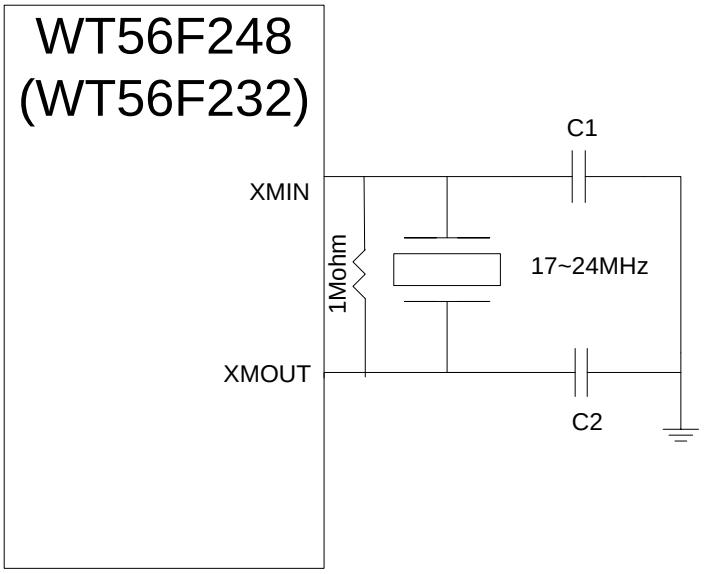
8.2.1 External 1~24 MHz Crystal Oscillator

Example

Crystal Oscillator	C1, C2 = 10pF ~ 33pF
Ceramic Resonator	C1, C2 = 10pF ~ 33pF

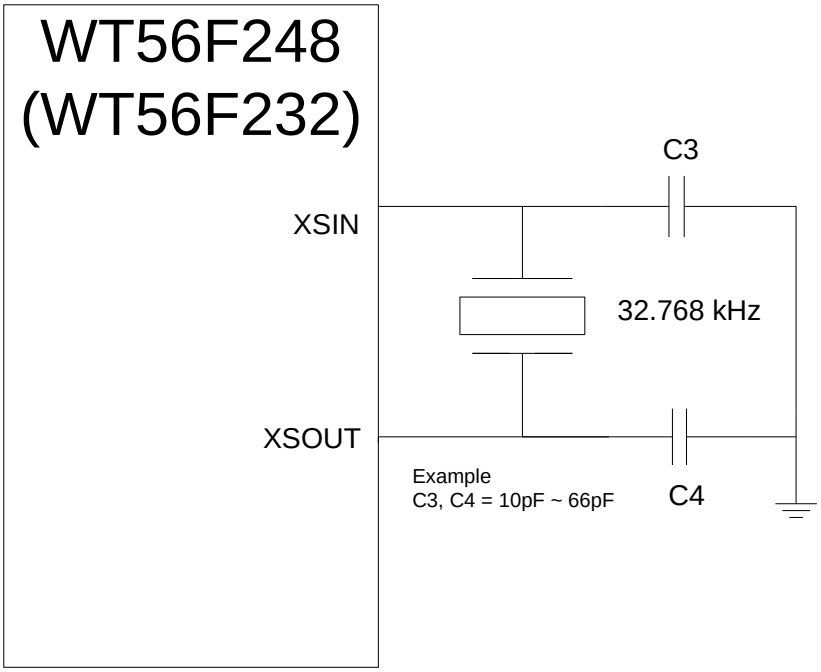
* The example load capactor value(C1,C2,C3,C4) is common value but may not be appropriate for some crystal or ceramic resonator.



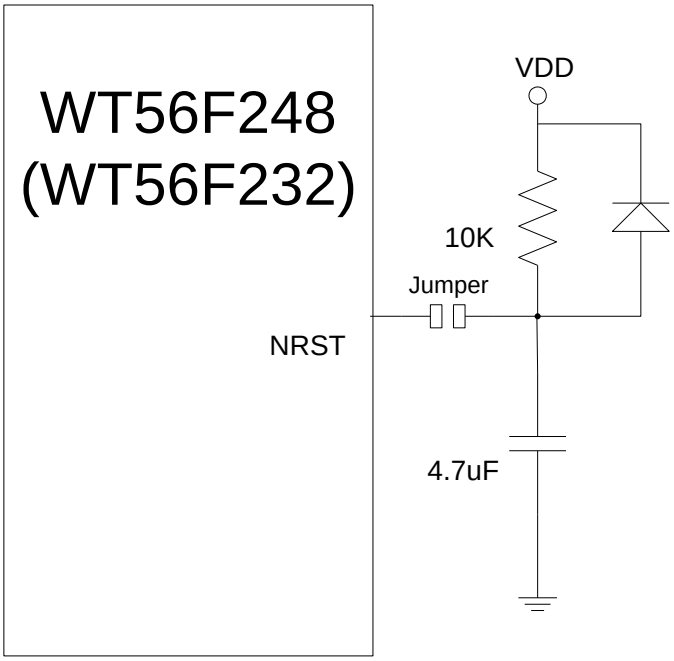


Note: WT56F248/232 has built-in internal RC oscillators, thus external crystal oscillators are not essential. If for more precise application, external crystal oscillator is available for use.

8.2.2 External 32.768 kHz Crystal Oscillator

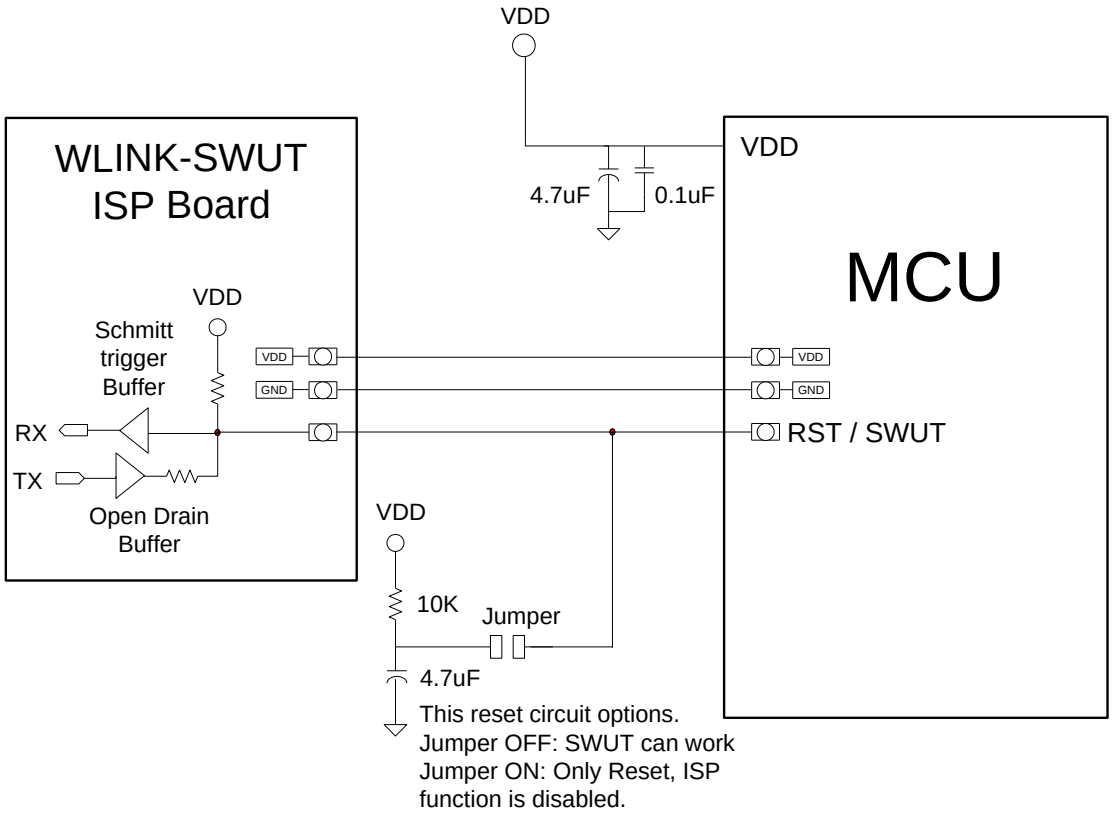


8.3 RESET Circuit

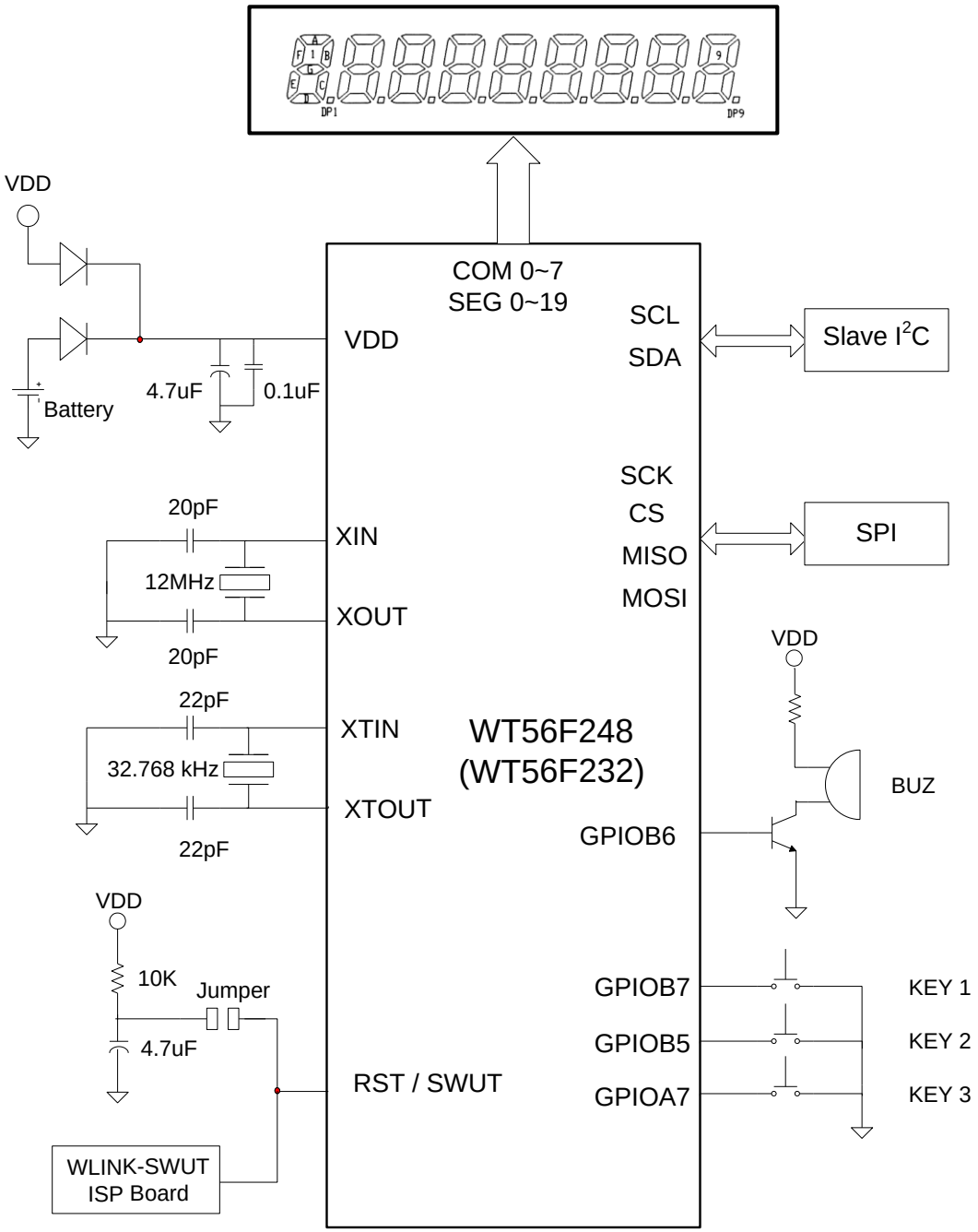


Note: Reset Circuit will influence programming process, and it requires adding **Jumper for isolation.**

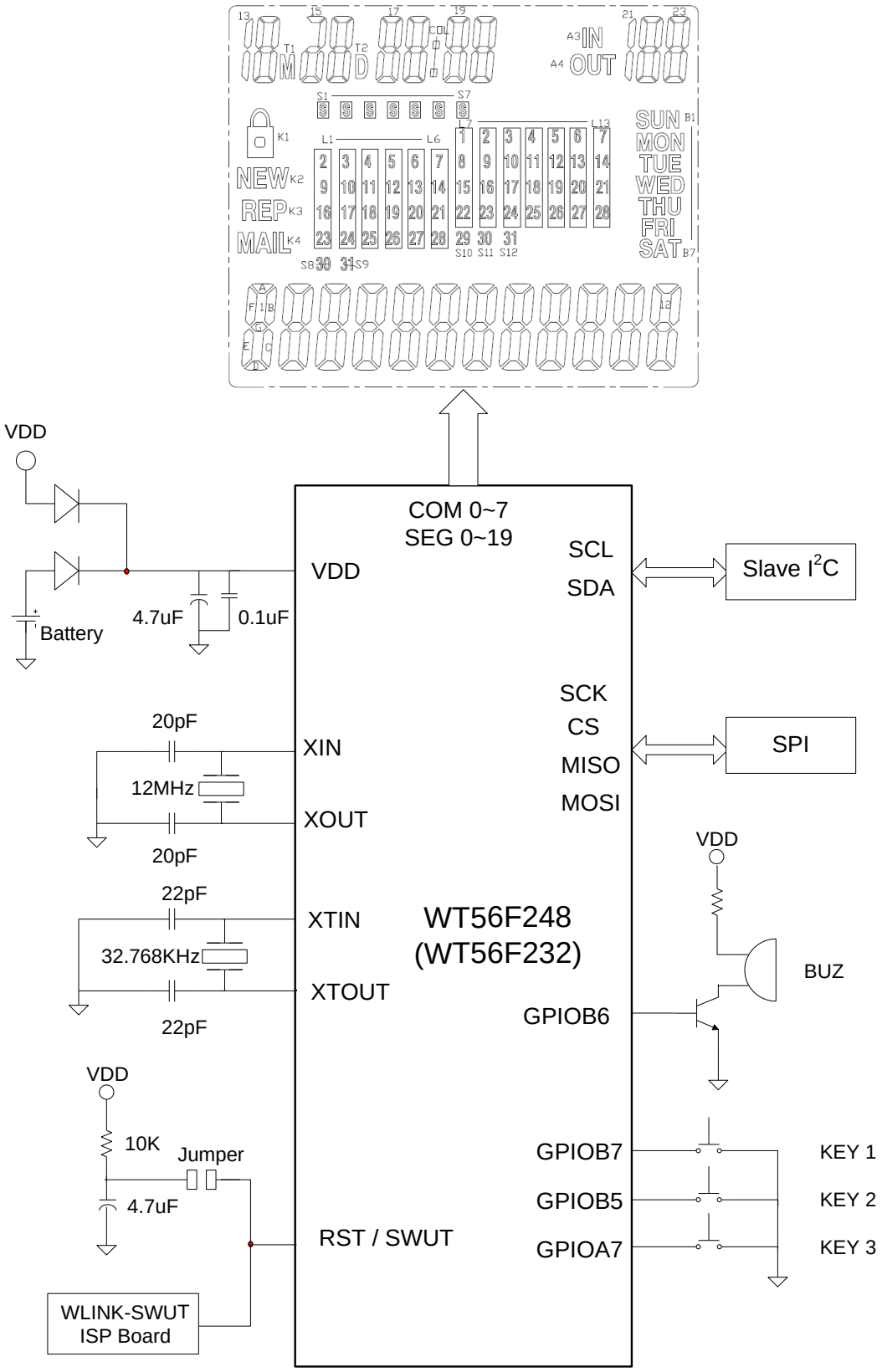
8.4 Standard Circuit



8.5 Development board circuits (4COM LCD)



8.6 Development board circuit (8COM LCD)



9. Product Naming Rule

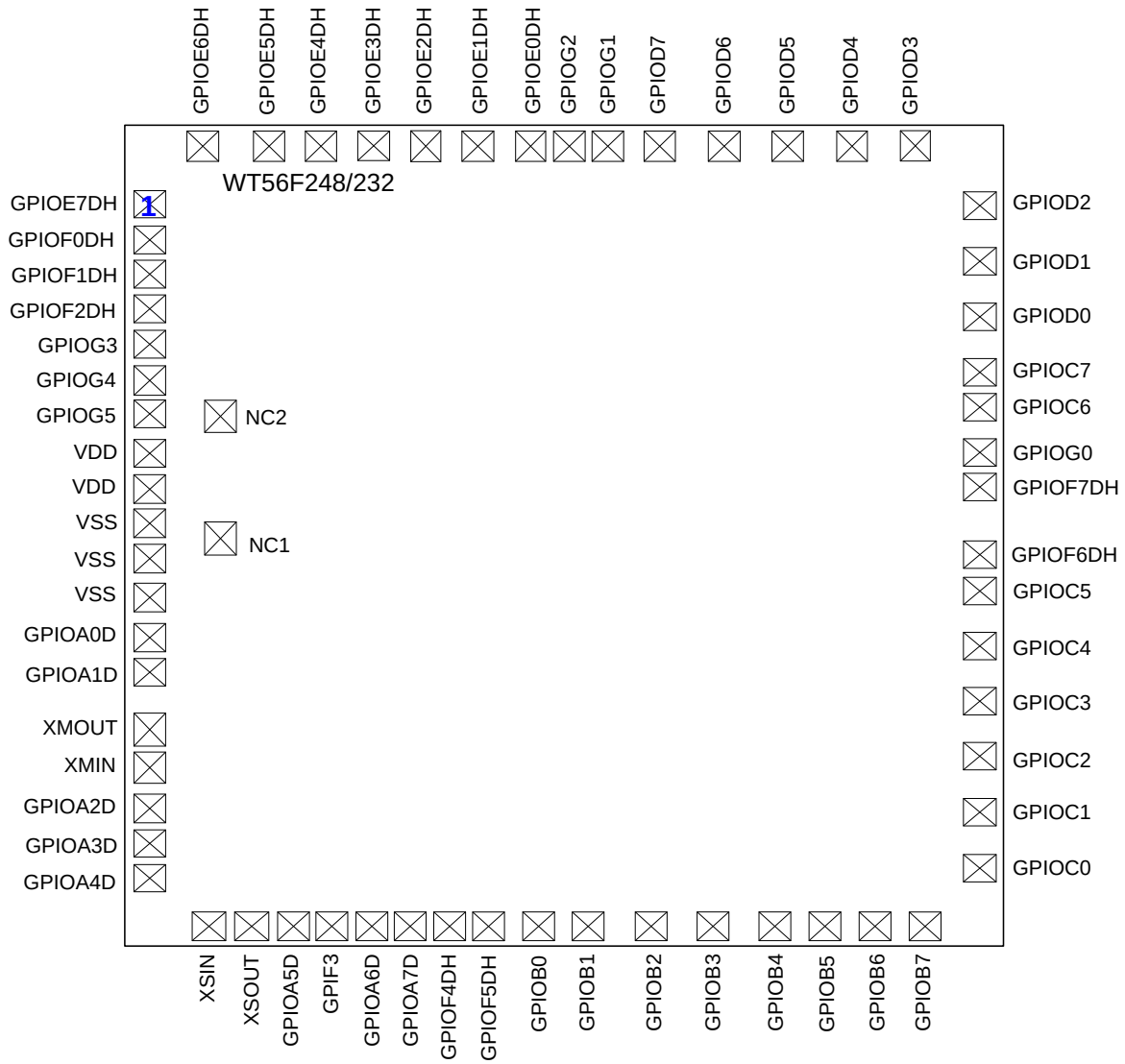
WT	Consumption market	LCD function	Seed code (Family)	Flash Size (K Bytes)		Remarks
WT	5	1F	1	0	4	5: MCU/DSP embedded, used in general-purpose or consumption market related product. 1X: 8-bit MCU 1F: Flash type 8-bit MCU without LCD function
			1	0	8	
			1	1	6	
			5	1	6	
WT	5	6F	1	0	8	5: MCU/DSP embedded, used in general-purpose or consumption market related product. 6X: LCD back light module controller 6F: Flash type 8-bit MCU with LCD function
			2	1	6	
			2	3	2	
			2	4	8	

10. Ordering Information

Package Type	Package Outline	Part Number
64-pin LQFP	7mil x 7mil	WT56F248-RG64AWT
44-pin LQFP	10mil x 10mil	WT56F248-RG44AWT
32-pin QFN	5mm x 5mm	WT56F248-UG32AWT
Wafer form or Chip form	-	WT56F248HXXXWT

Package Type	Package Outline	Part Number
64-pin LQFP	7mil x 7mil	WT56F232-RG64AWT
44-pin LQFP	10mil x 10mil	WT56F232-RG44AWT
32-pin QFN	5mm x 5mm	WT56F232-UG32AWT
Wafer form or Chip form	-	WT56F232HXXXWT

11. Pad Diagram & Location Table



No	Name	X	Y	No	Name	X	Y
1*	GPIOE7DH	46.45	1802.05	34	GPIOB6	1632.255	46.45
2*	GPIOF0DH	46.45	1717.05	35	GPIOB7	1742.255	46.45
3*	GPIOF1DH	46.45	1632.05	36*	GPIOC0	1863.55	188.745
4*	GPIOF2DH	46.45	1547.05	37*	GPIOC1	1863.55	323.745
5*	GPIOG3	46.45	1462.05	38*	GPIOC2	1863.55	458.745
6*	GPIOG4	46.45	1377.05	39*	GPIOC3	1863.55	593.745
7*	GPIOG5	46.45	1292.05	40*	GPIOC4	1863.55	728.745
8*	VDD	46.45	1195.51	41*	GPIOC5	1863.55	863.745
9*	VDD	46.45	1109.91	42*	GPIOF6DH	1863.55	948.745
10*	VSS	46.45	1024.91	43*	GPIOF7DH	1863.55	1113.745
11*	VSS	46.45	939.91	44*	GPIOG0	1863.55	1198.745
12*	VSS	46.45	845.05	45*	GPIOC6	1863.55	1308.745
13*	GPIOA0D	46.45	748.59	46*	GPIOC7	1863.55	1393.745
14*	GPIOA1D	46.45	663.59	47*	GPIOD0	1863.55	1528.745
15◎	XMOUT	46.45	525.45	48*	GPIOD1	1863.55	1663.745
16◎	XMIN	46.45	432.45	49*	GPIOD2	1863.55	1798.745
17*	GPIOA2D	46.45	332.95	50	GPIOD3	1722.045	1943.55
18*	GPIOA3D	46.45	247.95	51	GPIOD4	1582.545	1943.55
19*	GPIOA4D	46.45	162.95	52	GPIOD5	1443.045	1943.55
20※	XSIN	177.25	46.45	53	GPIOD6	1303.545	1943.55
21※	XSOUT	270.25	46.45	54	GPIOD7	1164.045	1943.55
22	GPIOA5D	359.255	46.45	55	GPIOG1	1049.545	1943.55
23	GPIF3	445.755	46.45	56	GPIOG2	964.545	1943.55
24	GPIOA6D	532.255	46.45	57	GPIOE0	879.545	1943.55
25	GPIOA7D	617.255	46.45	58	GPIOE1	765.045	1943.55
26	GPIOF4DH	702.255	46.45	59	GPIOE2	650.545	1943.55
27	GPIOF5DH	787.255	46.45	60	GPIOE3	536.045	1943.55
28	GPIOB0	897.255	46.45	61	GPIOE4	421.545	1943.55
29	GPIOB1	1007.255	46.45	62	GPIOE5	307.045	1943.55
30	GPIOB2	1142.255	46.45	63	GPIOE6	162.95	1943.55
31	GPIOB3	1277.255	46.45	64◎	NC1	200.45	1286.08
32	GPIOB4	1412.255	46.45	65◎	NC2	200.45	988.7
33	GPIOB5	1522.255	46.45				

Notes:

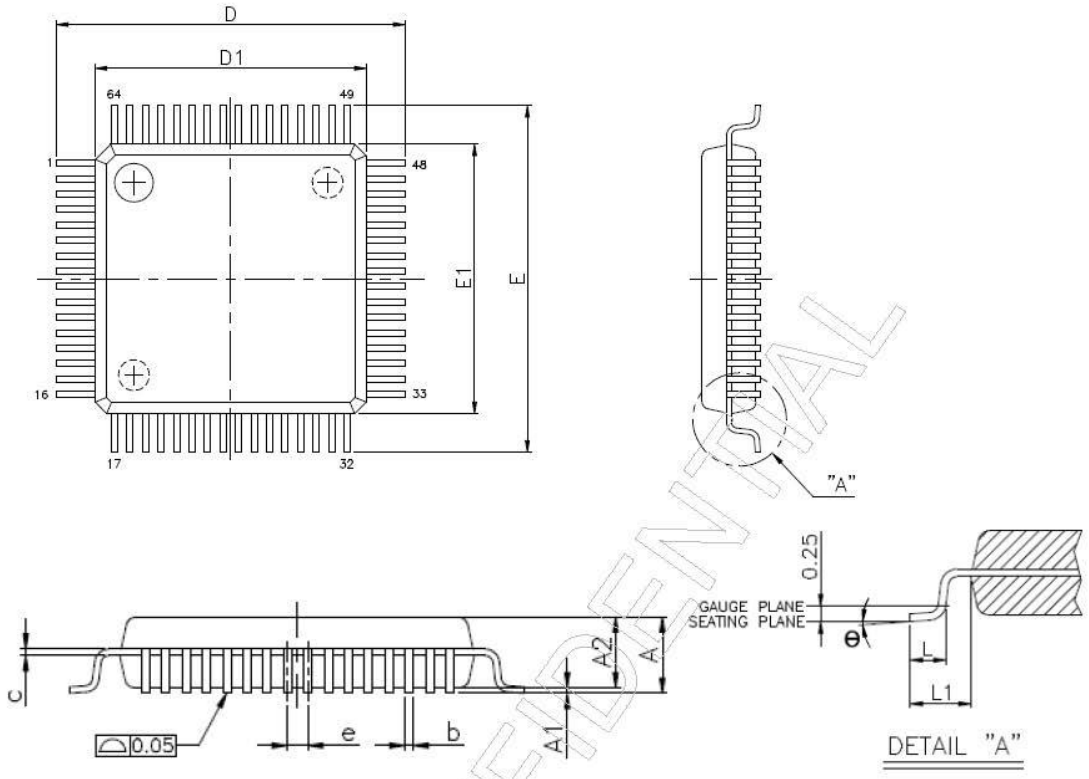
1. **The origin of pad location shown here is at lower-left corner of die.**
2. **PAD Window: (a) A type (◎): 66um x 73um**
   (b) B type (※): 73 um x 66um
   (c) C type (*): 66 um x 63um
   (d) D type ( ): 63 um x 66um
3. **To stabilize the supply voltages, please connect 0.1uF and 4.7uF bypass capacitors between VDD and VSS.**
4. **NC1 and NC2 pin, no connection for normal application.**
5. **All VDD pin need connect together. (No: 8, 9)**
6. **All VSS pin need connect together. (No: 10, 11, 12)**

12. Package Dimension

12.1 64-Pin LQFP

Low-Profile Quad Flat Package

LQFP-64 PIN



SYMBOLS	MIN	NOR	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	-	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ°	0	3.5	7

UNIT: mm

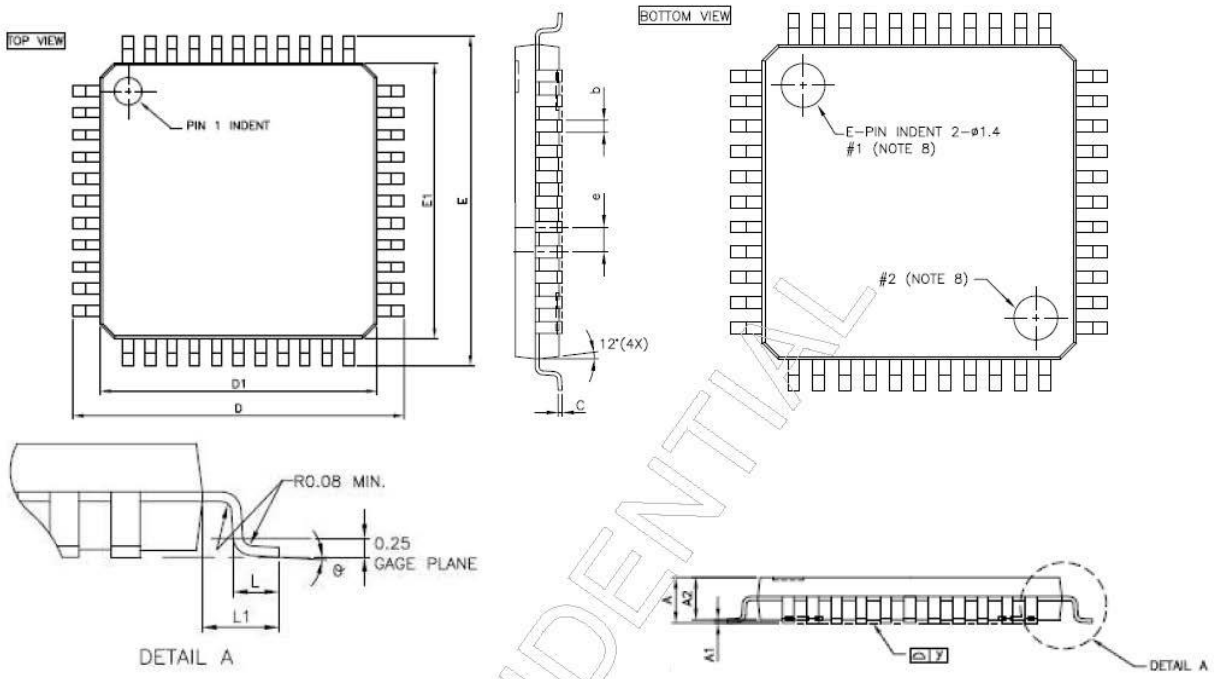
NOTES:
1. JEDEC outline : MS-026 BBD
2. Dimensions "D1" and "E1" do not include mold protrusion. Allowable protrusion is 0.25mm per side. "D1" and "E1" are maximum plastic body size dimensions including mold mismatch.
3. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" dimension by more than 0.08mm.

PREPARE	Cynthia	DATE: 2012/7/27
CHECK	Lawrence	DATE: 2012/7/27
APPROVE	Eric	DATE: 2012/7/27

12.2 44-Pin LQFP

Low-Profile Quad Flat Package

LQFP-44 PIN



SYMBOLS	MIN	NOR	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
C	0.09	-	0.20
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
e	-	0.80	-
L	0.45	0.60	0.75
L1	-	1.00	-
θ°	0	3.5	7
y	0.0	-	0.08

UNIT: mm

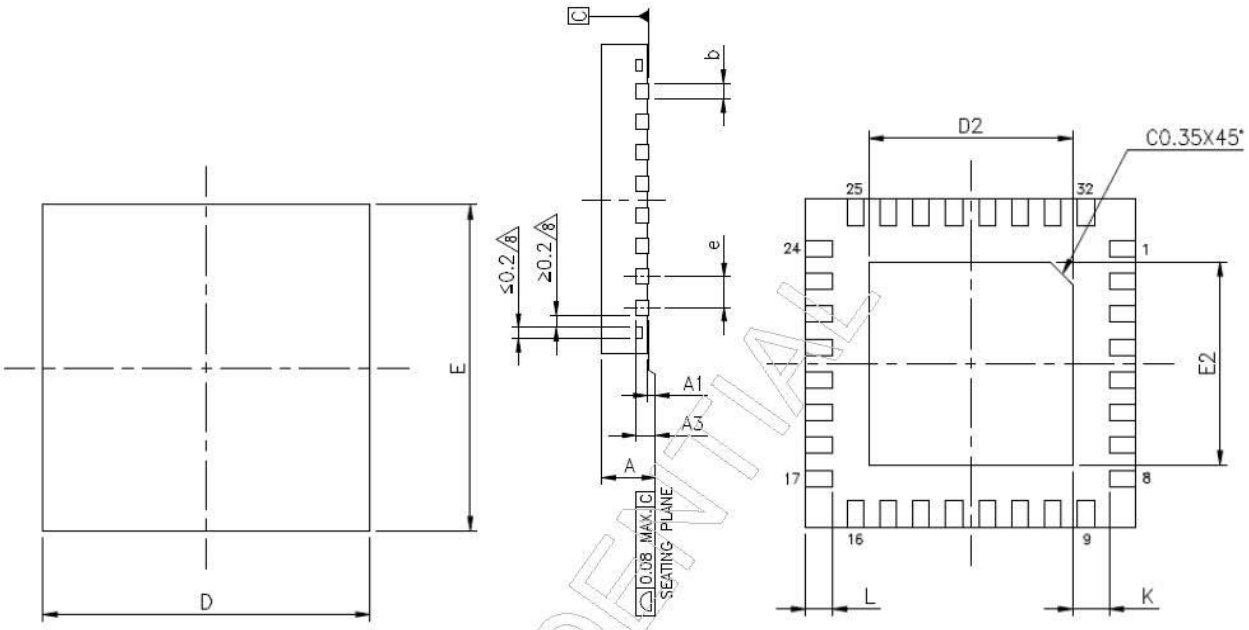
NOTES:
1. JEDEC outline: MS-026-BCB
2. Dimension "D1" and "E1" does not include mold protrusions. Mold protrusions shall not exceed 0.25mm per side.
3. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the "b" dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead to be 0.07mm.
4. Tolerance: ±0.25mm unless otherwise specified.
5. Otherwise dimension follow acceptable spec.

PREPARE	Cynthia	DATE: 2013/1/8
CHECK	Lawrence	DATE: 2013/1/8
APPROVE	Eric	DATE: 2013/1/8

12.3 32-Pin QFN

Quad Flat No-Lead Plastic Package

QFN-32 PIN



SYMBOLS	MIN	NOR	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	-	-
D2	3.10	3.20	3.25
E2	3.10	3.20	3.25

UNIT: mm

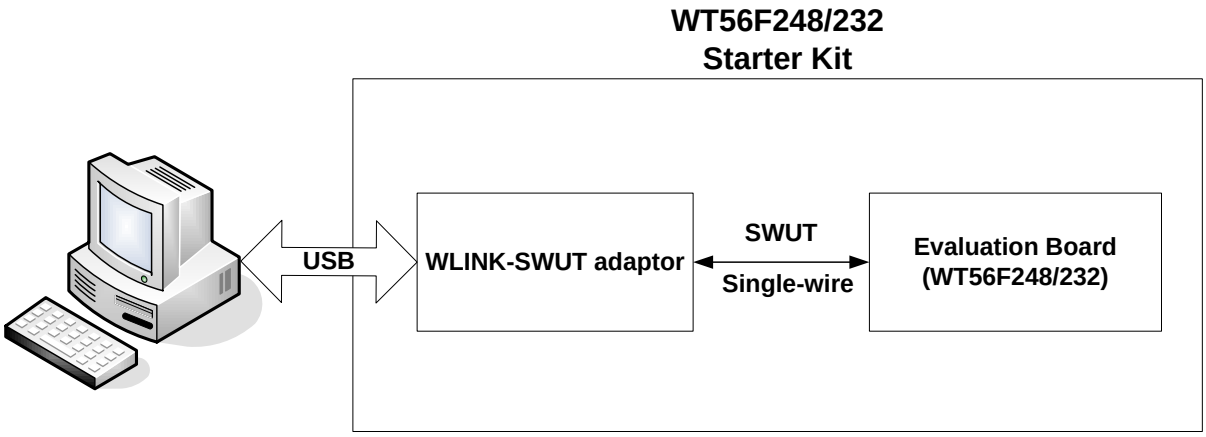
NOTES:
1. JEDEC outline : MO-220
2. Dimension "b" applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension "b" should not be measured in that radius area.
3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

PREPARE	Cynthia	DATE: 2012/8/1
CHECK	Lawrence	DATE: 2012/8/1
APPROVE	Eric	DATE: 2012/8/1

13. Development Tools

WT56F248/232 can work together with Keil C51 development environment. WLINK adaptor can link PC and WT56F248/232 evaluation board via ICE/ISP driver, and the debugger tools, demo board application software can perform In-Circuit Emulator (ICE) and In-system Programming (ISP) in Windows 98/2000/XP/Win7.

The development kits are illustrated in the figure below:



Development Tools List:

Please go to Weltrend's website http://www.weltrend.com.tw/ for more information.

Product Information	**General Purpose IC**	ADC Type MCU	WT51F104 Product Spec
			WT51F116/WT51F108 Product Spec
		ADC+LCD Type MCU	WT56F216 Product Spec
			WT56F108 Product Spec
			WT56F248/WT56F232 Product Spec
Technical Support	**Supporting Tools/ General Purpose IC**	ICE/ISP	**WA001** WLINK-SWUT Adapter
		Mass Production Programmer	**WA007 WLINK-SWUT-M4S**
		Mass Production Programmer Daughter Board	**WS001** WLINK-SWUT-M4S Daughter Board Support WT56F216/WT56F232/WT56F248 MCU RG44AWT LQFP 44 PKG
			WS003 WLINK-SWUT-M4S Daughter Board Support WT56F216 MCU SG28AWT SOP28 PKG
			WS004 WLINK-SWUT-M4S Daughter Board Support WT51F104/WT51F116/WT51F108 MCU OG20AWT SSOP20 PKG
			WS005 WLINK-SWUT-M4S Daughter Board Support WT51F104 MCU SG140WT SOP14 PKG SG080WT SOP8 PKG
			WS006 WLINK-SWUT-M4S Daughter Board Support WT51F104 MCU MG10AWT MSOP10 PKG
			WS007 WLINK-SWUT-M4S Daughter Board Support WT56F108 MCU RG64AWT LQFP64 PKG
			WS009 WLINK-SWUT-M4S Daughter Board Support WT51F116/WT51F108 MCU UG32AWT QFN32 PKG
			WS010 WLINK-SWUT-M4S Daughter Board Support WT51F116/WT51F108 MCU MG10BWT MSOP10 PKG
			WS011 WLINK-SWUT-M4S Daughter Board Support WT56F248/WT56F232 MCU RG64AWT LQFP64 PKG
			WS012 WLINK-SWUT-M4S Daughter Board Support WT56F248/WT56F232 MCU UG32AWT QFN32 PKG
			WS013 WLINK-SWUT-M4S Daughter Board Support WT56F108 MCU RG44AWT LQFP 44 PKG

			WS014 WLINK-SWUT-M4S Daughter Board Support WT56F108 MCU SG28AWT SOP28 PKG
Technical Support	**Supporting Tools/ General Purpose IC**	Evaluation Board	**WB000** WT56F216 EV Board
			WB001 WT51F104 EV Board
			WB005 WT56F216 Starter Kit Board
			WB006 WT51F104 Starter Kit Board
			WB007 WT56F108 Starter Kit Board
			WB008 WT51F116/WT51F108 Starter Kit Board (UG32AWT)
			WB010 WT56F248/WT56F232 Starter Kit Board
	Supporting Tools/ General Purpose IC	Starter Kit	**WK000** WT56F216 Starter Kit
			WK001 WT51F104 Starter Kit
			WK004 WT56F108 Starter Kit
			WK005 WT51F116/WT51F108 Starter Kit
			WK007 WT56F248/WT56F232 Starter Kit
	Technical Data/ General Purpose IC	WLINK Adapter Operation Manual	**Doc2** WLINK-SWUT Adapter Installation Manual
		Mass Production Programmer Operation Manual	**Doc26** WLINK-SWUT-M4S Operation Manual
		ICE/ISP Operation Manual	**Doc6** WLINK ICE Operation Manual (uVision IDE Version)
			Doc8 WLINK-SWUT ISP Operation Manual (for Alone Programmer)
		Evaluation Board Operation Manual	**Doc12** WT56F216 EV Board Operation Manual
			Doc13 WT51F104 EV Board Operation Manual
			Doc21 WT56F216 Starter Kit Quick Start Guide
			Doc22 WT51F104 Starter Kit Quick Start Guide
			Doc23 WT56F216 Starter Kit Operation Manual
			Doc24 WT51F104 Starter Kit Operation Manual
			Doc27 WT56F108 Starter Kit Operation Manual
			Doc28 WT51F116/WT51F108 Starter Kit Operation Manual
			Doc30 WT56F248/WT56F232 Starter Kit Operation Manual
		Mass Production ISP and Supplier Contact Information	**Doc20** Mass Production ISP Supplier

Technical Support	**Software Download/ General Purpose IC**	WLINK Adapter Driver	**SW2** WLINK-SWUT Adapter Driver
		Mass Production Programmer Driver	**SW2** WLINK-SWUT Adapter Driver
		ICE Driver/ISP Program	**SW6** WLINK-SWUT ICE Driver (for uVision IDE)
			SW8 WLINK-SWUT ISP Driver (for uVision IDE)
			SW9 WLINK-SWUT ISP Program (for Alone Programmer)
			SW17 Auto Install WLINK-SWUT ICE & ISP Driver (for uVision IDE) WLINK-SWUT ISP Driver (for uVision IDE)
		Example Program	**SW13** WT56F216 EV Board Example Program
			SW14 WT51F104 EV Board Example Program
			SW18 WT56F216 Starter Kit Board Example Program
			SW19 WT51F104 Starter Kit Board Example Program
			SW21 WT56F108 Starter Kit Board Example Program
			SW22 WT51F116/WT51F108 Starter Kit Board Example Program
			SW25 WT56F248/WT56F232 Starter Kit Board Example Program

14. Revision History

Version	History	Date
1.0	Initial issue	February 2018
1.01	Update Features & Electrical Characteristics (from -40℃ ~ +85℃ to -40℃ ~ +105℃)	June 2022
1.02	Update typos. CH 7.2: S/V -> μS /V CH 7.3: A -> μA CH 7.6: A -> μA CH 7.8: A -> μA; S -> μS CH 7.9: A -> μA; S -> μS CH 7.10: k -> kΩ	September 2022