WT51F516
Flash Memory Embedded 8-Bit General Purpose MCU

Data Sheet

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1. General Description

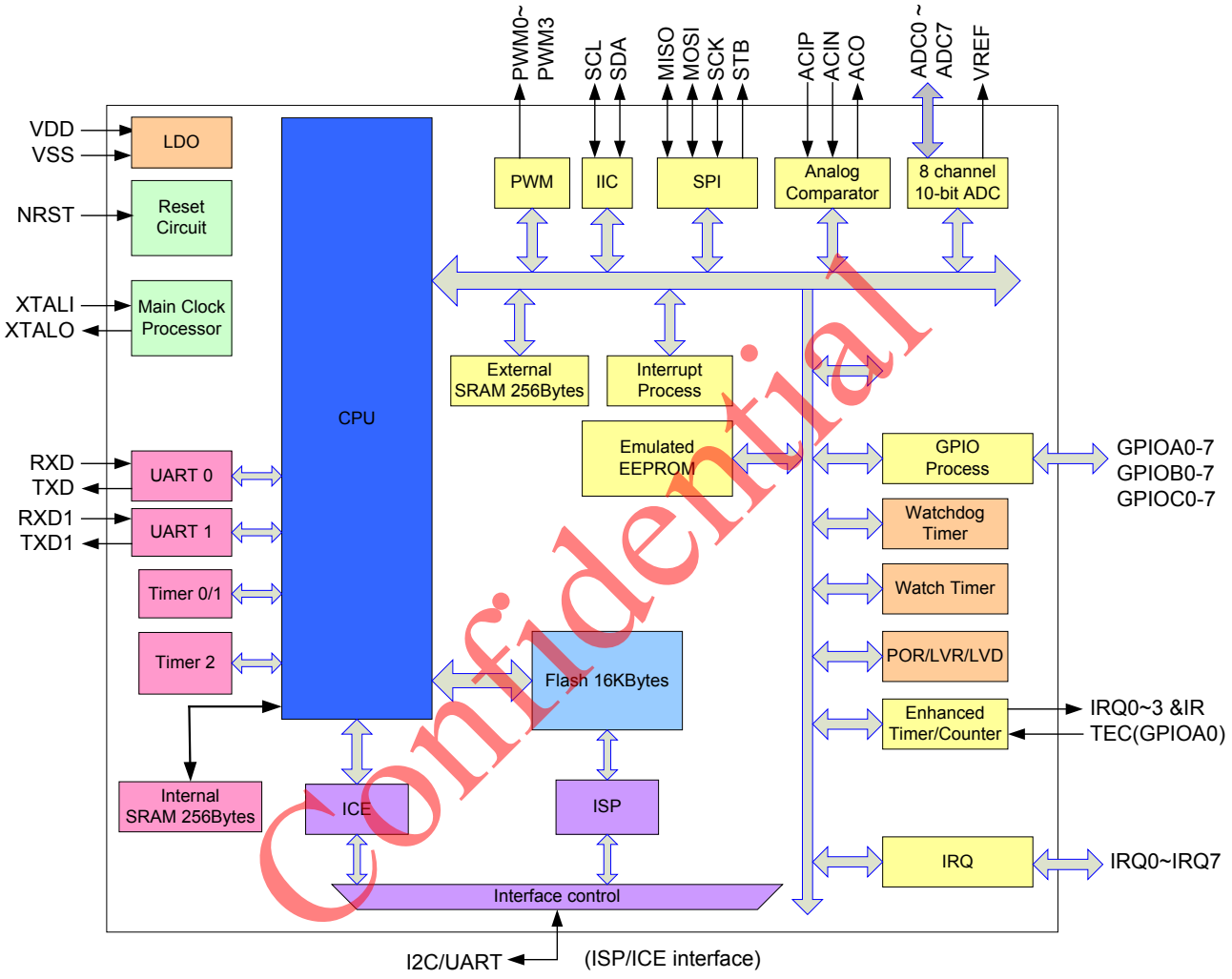
The WT51F516 is a high-performance 8-bit Microcontroller, which incorporates the 1T 8052 8-bit CPU operating up to 12 MHz. This chip has 16K bytes and 512 bytes SRAM. Its peripherals include 8-channel 10-bit ADC, one slave I^2C, one master/slave SPI, UART, four 10-bit PWMs, Hardware CEC, H/W universal IR receiver, Real Time Clock (RTC), Analog Comparator, Temperature Sensor, and Watchdog Timer (WDT). This chip also provides the capability to emulate E^2PROM by using the embedded flash memory. Power down mode and embedded ICE/ISP are also provided as well. The WT51F516 is suitable for a wide range of applications, including wireless applications such as Zigbee/RF4CE (one-to-one), consumer electronics such as helicopter model remote/motor control, home appliances, industrial control, LED lighting control, medical equipments, and PC peripherals.

2. Features

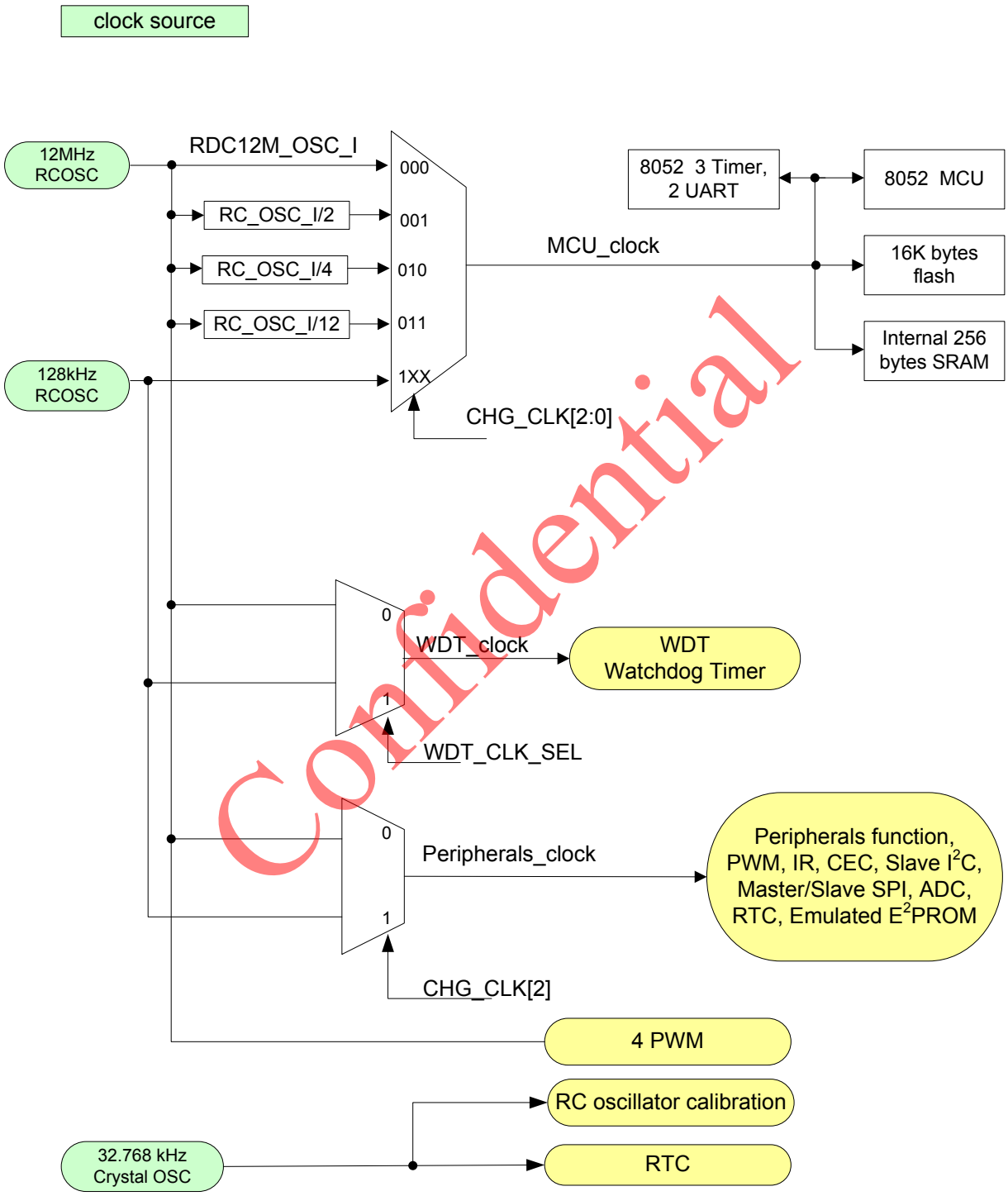
WT51F516 is an advanced 8052 Micro-controller, and it also provides the following features.

- 1T 8052 core, MCS-51 instruction set compatible
- Instruction execution time: Min. = 83.3ns @12 MHz
- 512 Bytes of RAM (256 Bytes of standard 8052 internal Data RAM and 256 Bytes of external RAM)
- 16K Bytes of flash memory for program storage
- Supporting Single Clock Oscillator:
  - Main Clock: Internal 12 MHz RC Oscillator
- Dual 16-bit Data Pointers (DPTR0 & DPTR1)
- Three 16-bit Timer/Counters (Timer0, Timer1, Timer2)
- One Watchdog Timer (WDT)
- One 16-bit Enhanced Timer with Capture function
- Two UARTs (UART0, UART1), support Baud rate 1200 bps ~ 230400 bps (at 12 MHz)
- 128 Bytes Emulated E^2PROM
- One master/slave SPI interface
- One slave I^2C interface
- Real Time Clock Module
- Infrared Receiver (IR)
- Consumer Electronics Control (CEC)
- Temperature Sensor
- Four 10-bit PWMs (PWM0, PWM1, PWM2, PWM3)
- 8-channel 10-bit Analog/Digital Converter (ADC0 ~ ADC8) with Voltage Reference source
- One Comparator
- Three power-saving modes: Sleep mode, Power-saving mode and Idle mode
- Four external Interrupt IRQ pins (IRQ0 ~ IRQ3)
- 24 programmable bi-directional I/O pins, 4 of them with both high current sink/source ability (10mA)
- Low Voltage Detection (LVD)
- On-chip Power On Reset (POR) and Low Voltage Reset (LVR)
- Built-in In-Circuit Emulator (ICE) and In-System Program (ISP)
- Operating voltage range: 2V ~ 5.5V
- Operating temperature: -40℃ ~ +85℃
- Dice & Package (Green Package): LQFP48, QFN32, SSOP20, and SOP16

3. Block Diagram



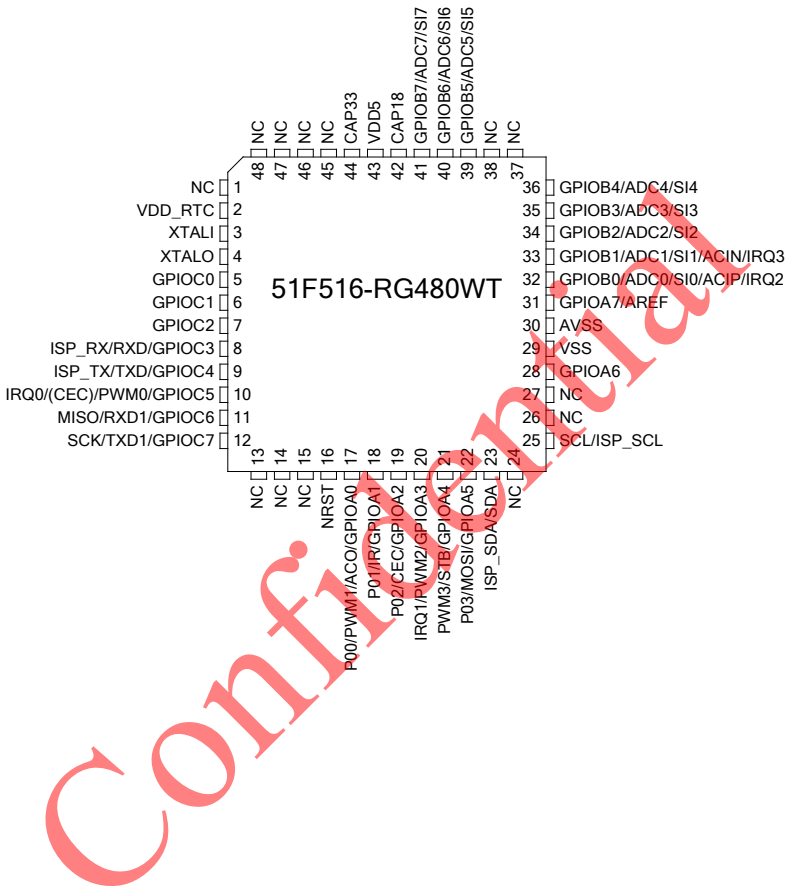
3.1 System Clock Tree



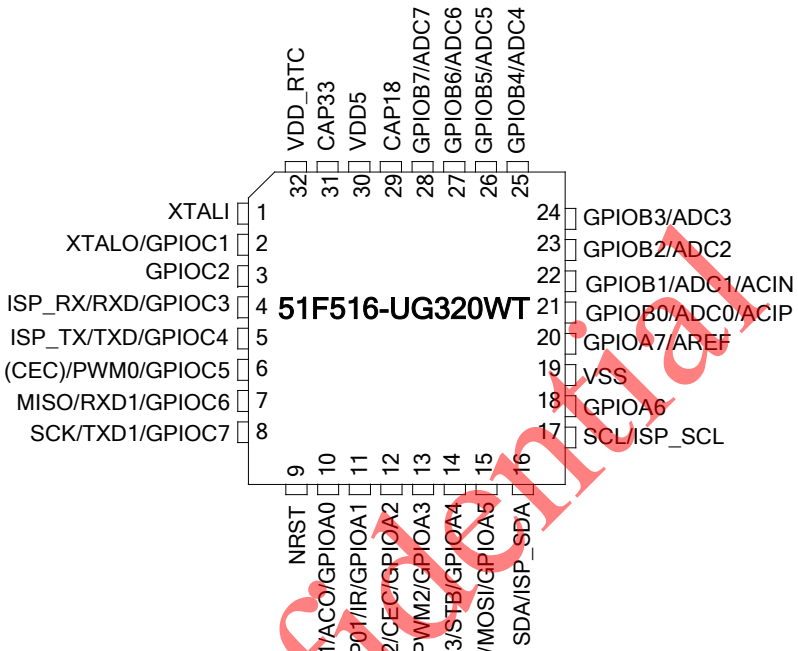
* **When using the external Crystal Oscillator, please select the corresponding driving ability according to its frequency. Refer to SYS System Control Register (XFR: 0x01 0x02) for more details.**

4. Pin Configuration

WT51F516-RG480WT 48-Pin LQFP

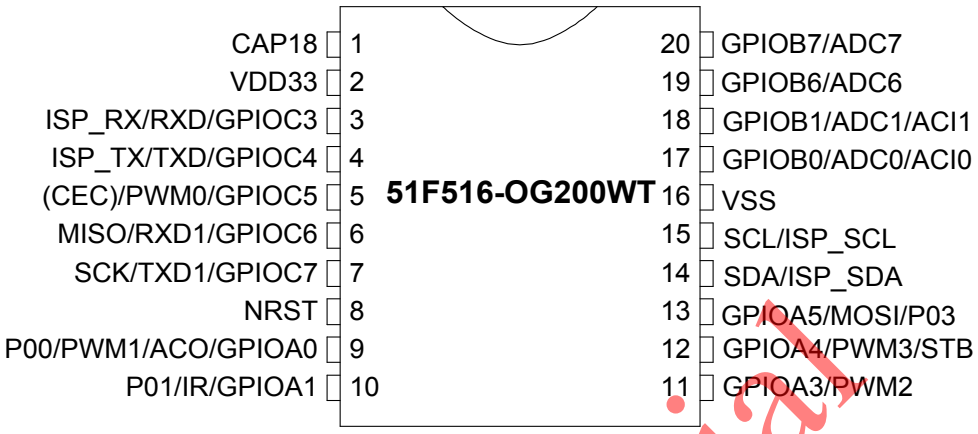


WT51F516-UG320WT 32-Pin QFN

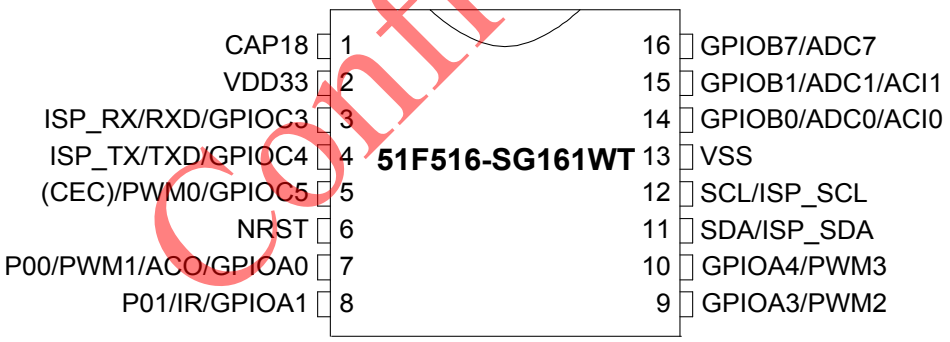


WT51F516-UG32AWT 32-Pin QFN

WT51F516-OG200WT 20-Pin SSOP



WT51F516-SG161WT 16-Pin SOP



4.1 Pin Function Description

4.1.1 48-Pin LQFP Pin Description

Pin Number					Pin Name		Primary Function
RG480	UG320/32A	OG200	SG161	DIE		I/O	Description
3	1			2	XTALI	I/O	32768 oscillator Input pin
4	2			3	XTALO	I/O	32768 oscillator Output pin
5				4	GPIOC0	I/O	GPIOC0: General-purpose I/O with programmable high current sink/source push-pull or open drain
6	2			5	GPIOC1	I/O	GPIOC1: General-purpose I/O with programmable high current sink/source push-pull or open drain
7	3			6	GPIOC2	I/O	GPIOC2: General-purpose I/O with programmable high current sink/source push-pull or open drain
8	4	3	3	7	GPIOC3/ RXD/ ISP_RXD	I/O	GPIOC3: General-purpose I/O with programmable high current sink/source push-pull or open drain RXD: UART Receive pin ISP_RXD: ISP RX pin
9	5	4	4	8	GPIOC4/ TXD/ISP_TXD	I/O	GPIOC4: General-purpose I/O with programmable high current sink/source push-pull or open drain TXD: UART Transmit pin ISP_TXD: ISP TX pin
10	6	5	5	9	GPIOC5/ PWM0/ CEC/ IRQ0	I/O	GPIOC5: General-purpose I/O with programmable high current sink/source push-pull or open drain PWM0: Pulse Width Modulation Output pin 0 CEC: Consumer Electronics Control Input pin IRQ0: External Interrupt input pin 0
11	7	6		10	GPIOC6/ RXD1/ MISO	I/O	GPIOC6: General-purpose I/O with programmable high current sink/source push-pull or open drain RXD1: UART Receive pin 1 MISO: MISO pin of SPI
12	8	7		11	GPIOC7/ TXD1/ SCK	I/O	GPIOC7: General-purpose I/O with programmable high current sink/source push-pull or open drain TXD1: UART Receive pin 1 SCK: SCK pin of SPI
16	9	8	6	12	NRES	I	Hardware Reset pin (active low)
17	10	9	7	13	GPIOA0/ PWM1/ ACO/ P00	I/O	GPIOA0: General-purpose I/O with programmable high current sink/source push-pull or open drain PWM1: Pulse Width Modulation Output pin 1 ACO: Comparator Output pin P00: Mapping to 8052 P0.0
18	11	10	8	14	GPIOA1/ IR/ P01	I/O	GPIOA1: General-purpose I/O with programmable high current sink/source push-pull or open drain IR: Infrared Receive pin P01: Mapping to 8052 P0.1
19	12			15	GPIOA2/ CEC/ P02	I/O	GPIOA2: General-purpose I/O with programmable high current sink/source push-pull or open drain CEC: Consumer Electronics Control Input pin P02: Mapping to 8052 P0.2

Pin Number					Pin Name		Primary Function
RG480	UG320/32A	OG200	SG161	DIE		I/O	Description
20	13	11	9	16	GPIOA3/ PWM2/ IRQ1	I/O	GPIOA3: General-purpose I/O with programmable high current sink/source push-pull or open drain PWM2: Pulse Width Modulation Output pin 2 IRQ1: External Interrupt Input pin 1
21	14	12	10	17	GPIOA4/ STB/ PWM3	I/O	GPIOA4: General-purpose I/O with programmable high current sink/source push-pull or open drain STB: STB pin of SPI PWM3: Pulse Width Modulation Output pin 3
22	15	13		18	GPIOA5/ MOSI/ P03	I/O	GPIOA5: General-purpose I/O with programmable high current sink/source push-pull or open drain MOSI: MOSI pin of SPI P03: Mapping to 8052 P0.3
23	16	14	11	19	SDA/ISP_SDA	I/O	SDA: Data pin of Slave I^2C ISP_SDA: Data pin of ISP
25	17	15	12	20	SCL/ISP_SCL	I/O	SCL: Clock pin of Slave I^2C ISP_SCL: ISP Clock pin
28	18			21	GPIOA6	I/O	GPIO A6: General-purpose I/O with programmable high current sink/source push-pull or open drain
29	19	16	13	22	VSS	PWR	Ground
29	19	16	13	23	VSS	PWR	Ground
29	19	16	13	24	VSS	PWR	Ground
30	19	16	13	25	AVSS	PWR	Ground for ADC
31	20			26	GPIOA7/ AREF	I/O	GPIOA7: General-purpose I/O with programmable high current sink/source push-pull or open drain AREF: ADC Reference Voltage Input pin
32	21	17	14	27	GPIOB0/ ADC0/ ACIP/ IRQ2	I/O	GPIOB0: General-purpose I/O with programmable high current sink/source push-pull or open drain ADC0: Analog/Digital Converter Input 0 ACIP: Comparator Input pin (+) IRQ2: External Interrupt Input pin 2
33	22	18	15	28	GPIOB1/ ADC1/ ACIN/ IRQ3	I/O	GPIOB1: ADC1: Analog/Digital Converter Input 1 ACIN: Comparator Input pin (-) IRQ3: External Interrupt Input pin 3
34	23			29	GPIOB2/ ADC2	I/O	GPIOB2: General-purpose I/O with programmable high current sink/source push-pull or open drain ADC2: Analog/Digital Converter Input 2
35	24			30	GPIOB3/ ADC3	I/O	GPIOB3: General-purpose I/O with programmable high current sink/source push-pull or open drain ADC3: Analog/Digital Converter Input 3
36	25			31	GPIOB4/ ADC4	I/O	GPIOB4: General-purpose I/O with programmable high current sink/source push-pull or open drain ADC4: Analog/Digital Converter Input 4
				32	NC		
39	26			33	GPIOB5/ ADC5	I/O	GPIOB5: General-purpose I/O with programmable high current sink/source push-pull or open drain

Pin Number					Pin Name		Primary Function
RG480	UG320/32A	OG200	SG161	DIE		I/O	Description
							ADC5: Analog/Digital Converter Input 5
40	27	19		34	GPIOB6/ ADC6	I/O	GPIOB6: General-purpose I/O with programmable high current sink/source push-pull or open drain ADC6: Analog/Digital Converter Input 6
41	28	20	16	35	GPIOB7/ ADC7	I/O	GPIOB7: General-purpose I/O with programmable high current sink/source push-pull or open drain ADC7: Analog/Digital Converter Input 7
				36	NC		
42	29	1	1	37	CAP18	PWR	1.8V LDO Filter
42	29	1	1	38	CAP18		
43	30	2	2	39	VDD5	PWR	5V Power
44	31	2	2	40	CAP33		3.3V LDO Filter
44	31	2	2	41	CAP33	PWR	
				42	NC		
2	32	2	2	1	VDD_RTC	PWR	RTC 3.3V Power

(a) All GPIOs use Schmitt trigger input.

(b) While using Slave I^2C or UART, the external circuit needs pull high resistor.

(c) The MAX input for GPIOA7, GPIOB7~0, GPIOC1 and XTALI is +3.6V, and the other GPIOs MAX input is +5.5V.

(d) CEC pin shared with GPIOA2/GPIOC5 depends on CEC_IO_SLT Register (Index 02H-bit4).

4.2 Pin Description

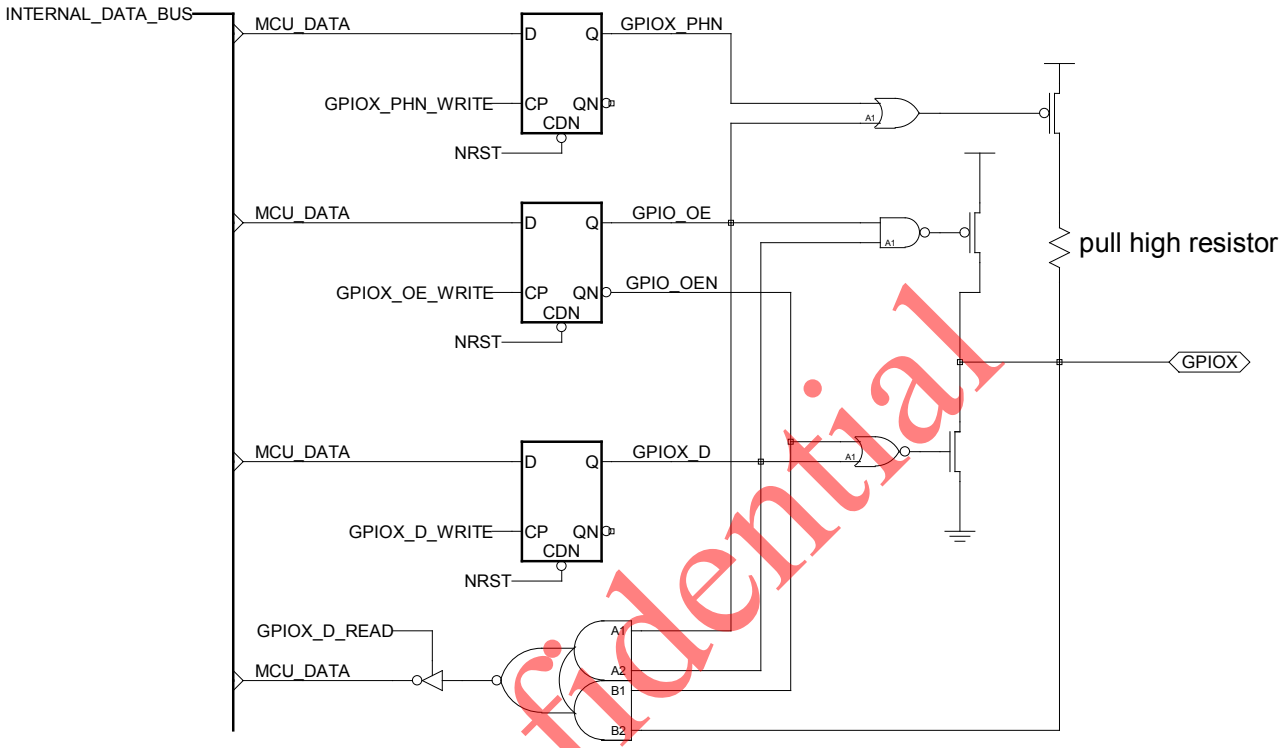
Explain each pin function in details.

Pin Name	Type	Description
PORT		
GPIOA0 ~ GPIOA7	I/O	8-bit bidirectional general-purpose I/O port
GPIOB0 ~ GPIOB7	I/O	8-bit bidirectional general-purpose I/O port
GPIOC0 ~ GPIOC7	I/O	8-bit bidirectional general-purpose I/O port
IRQ		
IRQ0 ~ IRQ3	I	4 External Interrupt Request Input pins
PWM		
PWM0	O	PWM 0 Output
PWM1	O	PWM 1 Output
PWM2	O	PWM 2 Output
PWM3	O	PWM 3 Output
UART		
RXD	I	UART0 Receive
TXD	O	UART0 Transmit

Pin Name	Type	Description
RXD1	I	UART1 Receive
TXD1	O	UART1 Transmit
SPI		
SCK	I/O	SPI interface clock
MOSI	I/O	SPI Data pin MOSI (Master Output; Slave Input)
STB	O	SPI Enable
MISO	I/O	SPI Data pin MISO (Master Input; Slave Output)
ADC		
ADC0 ~ ADC7	I	8 Analog/Digital Input pin
ACOMP		
ACIP	I	Comparator Positive Input pin
ACIN	I	Comparator Negative Input pin
ACO	O	Comparator Output pin
I²C		
SCL	I/O	I²C interface clock
SDA	I/O	I²C interface data
VCC & VSS		
VDD	P	Power
VSS	P	Ground
OSC		
XTALO	O	Main crystal oscillator output
XTALI	I	Main crystal oscillator input
RESET		
NRST	I	CPU reset
ISP & ICE		
I^2C	I/O	ISP & ICE interface

4.3 Port Structure

I/O Structure



5. Normal Function

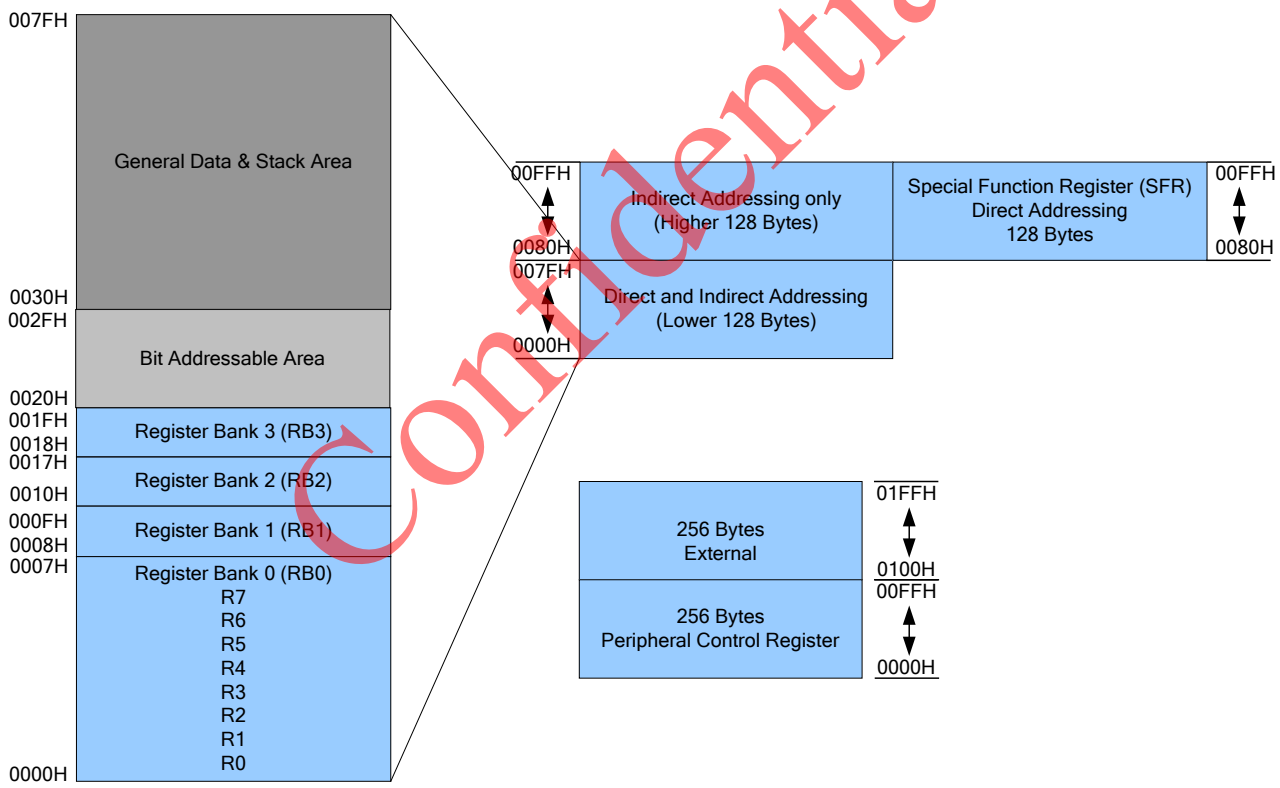
5.1 CPU

The WT51F516 has an embedded 8-bit 1T 8052 compatible CPU with 16-bit space addressable and 8-bit data access functions. The instruction execution time of 1T 8052 is three times faster than that of the conventional 3T 8052, and 12 times faster than that of 12T 8052. All of the functions and Special Function Register (SFR) definitions will be described in below sections.

5.2 RAM

The WT51F516 consists of 256+256 Bytes of SRAM. The 256 Bytes of RAM is the internal RAM of the common 8052. External 256 Bytes of SRAM can be accessed by the execution of MOVX instruction.

Below figure shows a map of the RAM. For Peripheral Control Registers, see section 6.1.



The internal SRAM contains:
128 Bytes of internal SRAM, locates from 0x0000H to 0x007FH (direct and indirect addressing is allowed)
128 Bytes of internal SRAM, locates from 0x0080H to 0x00FFH (indirect addressing)
256 Bytes of external SRAM, locates from 0x0100H to 0x01FFH (accessed by MOVX instruction)
Its main purpose is for storing data in the program, and therefore it is also called Data Memory. The Data memory of WT51F516 includes the following sections:

(1) The lower 128 bytes of internal SRAM (0000H ~ 007FH) which can be accessed by direct or indirect addressing is divided into 3 segments:

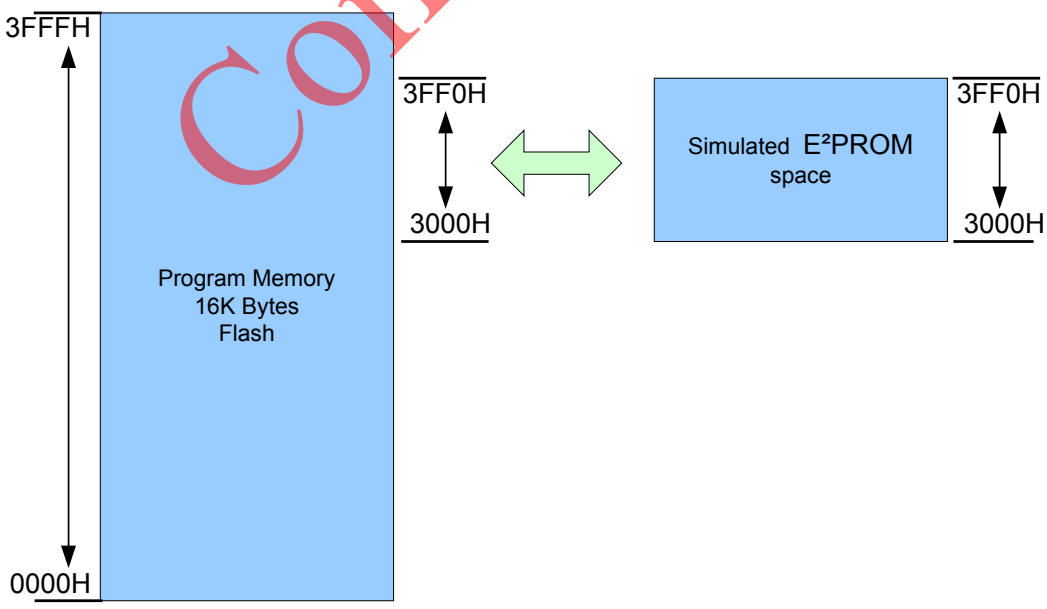
- **General Purpose Register**: Locates from 0000H to 001FH, 32 Bytes in total, can be divided into four register banks. Each register bank contains eight general purpose registers (R0~R7). Four register banks can be selected by the select bit RS1 and RS0 in the Program Status Word Register.
- **Bit Addressable Area**: Locates from 20H to 2FH, 16 Bytes in total. Each one of the 128 bits of this segment can be directly addressed by Bit Addressing.
- **General Data Area:** Locates from 0030H to 007FH, 80 Bytes are available to the user as data RAM (including the Stack area).

(2) The higher 128 bytes of internal SRAM (0080H ~ 00FFH) can be accessed by indirect addressing through R0 or R1 (*).
(3) Special Function Registers (SFR), locates from 0080H to 00FFH, can be accessed by direct addressing (*).
(4) 128 Bytes of external SRAM, locates from 0100H to 00FFH, can be accessed by instruction MOVX.
(*) Although the SFR and the higher 128 Bytes of internal RAM occupy the same addresses (0080H ~ 00FFH), they are two separate areas. MCU will automatically determine which area is in use by two different accessing ways.

5.3 Flash Memory

The WT51F516 consists of 16K built-in flash, which can be served as general Program memory or simulated E^2PROM (0x3000H ~ 0x3FF0H) with features as below:

- FLASH memory: 16K Bytes
- Operating voltage: 2V ~ 5.5V
- In-System Programming (ISP)
- Over 10 years Data Retention
- Emulated E^2PROM function



5.4 Memory Mapping

WT51F516 built-in 128 Bytes of direct addressing 8052 standard Special Function Register (SFR), as described below.

- CPU Core Register: ACC, B, PSW, SP, DPL0, DPH0, DPL1, DPH1, DPS
- Interrupt Register: IP, IE, XICON
- I/O port Register: P0
- Timer Register: TCON, TMOD, TL0, TH0, TL1, TH1, T2CON, T2MOD, TL2, TH2, RCAP2L, RCAP2H
- UART0 Register: SCON0, SBUF0, SBRG0H, SBRG0L, PCON
- UART1 Register: SCON1, SBUF1, SBRG1H, SBRG1L

Special Function Register (SFR) MAP:

	Bit Addressable	No Bit Addressable							
F8H									FFH
F0H	B								F7H
E8H									EFH
E0H	ACC								E7H
D8H	SCON1	SBUF1	SBRG1H	SBRG1L					DFH
D0H	PSW								D7H
C8H	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2			CFH
C0H	XICON								C7H
B8H	IP								BFH
B0H									B7H
A8H	IE								AFH
A0H									A7H
98H	SCON0	SBUF0	SBRG0H	SBRG0L					9FH
90H									97H
88H	TCON	TMOD	TL0	TL1	TH0	TH1			8FH
80H	*P0*	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON	87H

Special Function Register (SFR) Table:

Register Name	Address	Reset Value	Description
P0	80H	FFH	Port 0
SP	81H	07H	Stack Pointer
DPL	82H	00H	Data Pointer 0 low byte
DPH	83H	00H	Data Pointer 0 high byte
DPL1	84H	00H	Data Pointer 1 low byte
DPH1	85H	00H	Data Pointer 1 high byte
DPS	86H	00H	Data Pointer select
PCON	87H	40H	Power Control Register
TCON	88H	00H	Timer 0/1 Counter Control

Register Name	Address	Reset Value	Description
TMOD	89H	00H	Timer 0/1 Mode Control
TL0	8AH	00H	Timer 0, low byte
TL1	8BH	00H	Timer 1, low byte
TH0	8CH	00H	Timer 0, high byte
TH1	8DH	00H	Timer 1, high byte
SCON0	98H	00H	Serial Port 0, Control Register
SBUF0	99H	00H	Serial Port 0, Data Buffer
SBRG0H	9AH	00H	Serial Baud rate Generator, high byte
SBRG0L	9BH	00H	Serial Baud rate Generator, low byte
IE	A8H	00H	Interrupt Enable Register
IP	B8H	00H	Interrupt Priority Register 1
XICON	C0H	00H	Interrupt Enable Register (INT2/INT3)
T2CON	C8H	00H	Timer 2 Control
T2MOD	C9H	00H	Timer 2 Mode Control
RCAP2L	CAH	00H	Compare/Reload/Capture Register, low byte
RCAP2H	CBH	00H	Compare/Reload/Capture Register, high byte
TL2	CCH	00H	Timer 2, low byte
TH2	CDH	00H	Timer 2, high byte
PSW	D0H	00H	Program Status Word
SCON1	D8H	00H	Serial Port 1, Control Register
SBUF1	D9H	00H	Serial Port 1, Data Buffer
SBRG1H	DAH	00H	Serial Baud rate Generator 1, high byte
SBRG1L	DBH	00H	Serial Baud rate Generator 1, low byte
ACC	E0H	00H	Accumulator
B	F0H	00H	B Register

Note: Refer to 5.7 "Reset" section for the initial value of SFR.

Introduction of WT51F516 CPU SFR is as below:

B: Address: F0H **Reset Value: 0x00**

7	6	5	4	3	2	1	0
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

The B register is used during multiply and divide operations. It can store the multiplier and the high bytes of operation result in multiply operation, and also the divisor and the remainder of operation result in divide operation. The B register can be used as a general register.

ACC: Address: E0H **Reset Value: 0x00**

7	6	5	4	3	2	1	0
ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

ACC is the Accumulator register, used for data operations.

0: Address: 80H **Reset Value: 0xFF**

7	6	5	4	3	2	1	0
				P0.3	P0.2	P0.1	P0.0

Data setting of Output/Input port P0.

PSW (Program Status Word): Address: D0H **Reset Value: 0x00**

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	F1	PARITY

The Program Status Word contains program status information.

Bit Number	Bit Mnemonic	Description
7	CY	Carry Flag, used to indicate the result of arithmetic operation whether a carry or borrow occurred in the 7th bit. Operation result of Addition: 1: a carry occurred; 0: no carry occurred. Operation result of Subtraction: 1: a carry occurred; 0: no carry occurred.
6	AC	Auxiliary-Carry Flag, used to indicate the result of arithmetic operation whether the 3rd bit borrow (or carry) from the 4th bit occurred. Operation result of Addition: 1: a carry occurred; 0: no carry occurred. Operation result of Subtraction: 1: a carry occurred; 0: no carry occurred.
5	F0	General-purpose Flag, can be served as common read/write bit.
4	RS1	Register Bank Select bits 1 and 0 (refer to Register Bank Selection Table).
3	RS0	
2	OV	Overflow Flag, used to indicate the result of arithmetic operation whether an overflow occurred. If OV = 1, an overflow occurred. Otherwise, it is cleared.
1	F1	General-purpose Flag, can be served as common read/write bit.
0	P	Parity Flag. It is set to indicate an odd number of “1” bits in the accumulator. Otherwise, it is cleared.

Register Bank Selection Table:

Register Bank	Address	RS1	RS0
0	00H-07H	0	0
1	08H-0FH	0	1
2	10H-17H	1	0
3	18H-1FH	1	1

SP (Stack Point) Address: 81H **Reset Value: 0x07**

7	6	5	4	3	2	1	0
SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Stack Pointer, indicated the location at which the last byte was pushed onto the stack. It is incremented before data is stored during PUSH.

DPL0 (DPTR0, low byte of the 16-bit data pointer) Address: 82H **Reset Value: 0x00**

7	6	5	4	3	2	1	0
DPL0.7	DPL0.6	DPL0.5	DPL0.4	DPL0.3	DPL0.2	DPL0.1	DPL0.0

DPL0 is a low byte of DPTR0, using together with the data pointer of DPH0.

DPH0 (DPTR0, high byte of the 16-bit data pointer) Address: 83H **Reset Value: 0x00**

7	6	5	4	3	2	1	0
DPH0.7	DPH0.6	DPH0.5	DPH0.4	DPH0.3	DPH0.2	DPH0.1	DPH0.0

DPH0 is a high byte of DPTR0, using together with the data pointer of DPL0.

DPL1 (DPTR1, low byte of the 16-bit data pointer 1) Address: 84H **Reset Value: 0x00**

7	6	5	4	3	2	1	0
DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0

DPL1 is low byte of DPTR1, using together with the data pointer of DPH1.

DPH1 (DPTR1, high byte of the 16-bit data pointer 1) Address: 85H **Reset Value: 0x00**

7	6	5	4	3	2	1	0
DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0

DPH1 is a high byte of DPTR1, using together with the data pointer of DPL1.

DPS (Data point select) Address: 86H **Reset Value: 0x00**

7	6	5	4	3	2	1	0
							DPS

Data Point selection: If DPS = 0, selects DPTR0 (DPH0, DPL0)
If DPS = 1, selects DPTR1 (DPH1, DPL1)

Note: Other special function registers will be discussed in later sections.

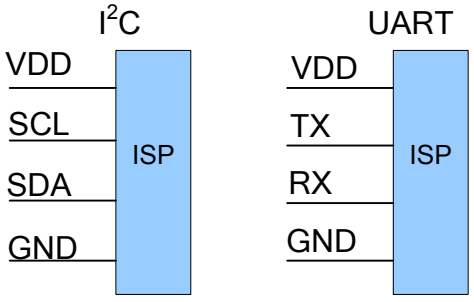
5.5 In-System Programming (ISP)

In-System Programming function allows users to program the target board directly without removing any components.

ISP interface adopts:

4-wire: VDD, GND (VSS), SCL, SDA
4-wire: VDD, GND (VSS), TX, RX

The figure below illustrates pins of ISP interface:



Note: See WT51F516 ISP/ICE User's Manual for more details.

5.6 Timer

The WT51F516 contains three 16-bit Timers (Timer0 ~ 2). All three Timers can be configured as Timer or Counter.

5.6.1 Timer0 & Timer1 (Timer 0/1)

The internal Timer 0 and Timer 1 of WT51F516 have four operation modes to be selected by bits M11, M10, or M01, and M00 respectively in the Special Function Register TMOD, as described below.

TMOD (8052 Timer0/1 Mode Control Register) Address: 89H

7	6	5	4	3	2	1	0
GATE1	C1/T1	M11	M10	GATE0	C0/T0	M01	M00

Bit Number	Bit Mnemonic	Description
7	GATE1	GATE1 = 1, invalid GATE1 = 0, configured as internal Timer. If TR1 = 1, Timer1 starts.
6	C1/T1	Timer selector C1/T1 = 1, invalid C1/T1 = 0, configured as an internal Timer, and the counter signal is from MCU Clock 12 MHz IRC ÷ 12
5-4	M11-M10	Timer 1 mode selection bits 00: Mode 0, 13-bit Timer 01: Mode 1, 16-bit Timer 10: Mode 2, 8-bit auto-reload Timer 11: Mode 3, Timer 1 stopped and retained count.
3	GATE0	GATE0 = 1, invalid GATE0 = 0, configured as an internal Timer. If TR0 = 1, Timer 0 starts.
2	C0/T0	Timer selector C0/T0 = 1, invalid C0/T0 = 0, configured as internal Timer, and the counter signal is from MCU Clock 12 MHz IRC ÷ 12
1-0	M01-M00	Timer 0 mode selection bits 00: Mode 0, 13-bit Timer 01: Mode 1, 16-bit Timer 10: Mode 2, 8-bit auto-reload Timer 11: Mode 3, 8-bit Timer (TL0 uses TR0 bit and TH0 uses TR1 bit)

Note: When use Timer 0 & Timer 1, Cx/Tx must be set as "0" and then Timer can work normally.

TCON (8052 Timer 0/1 Control Register) Address: 88H

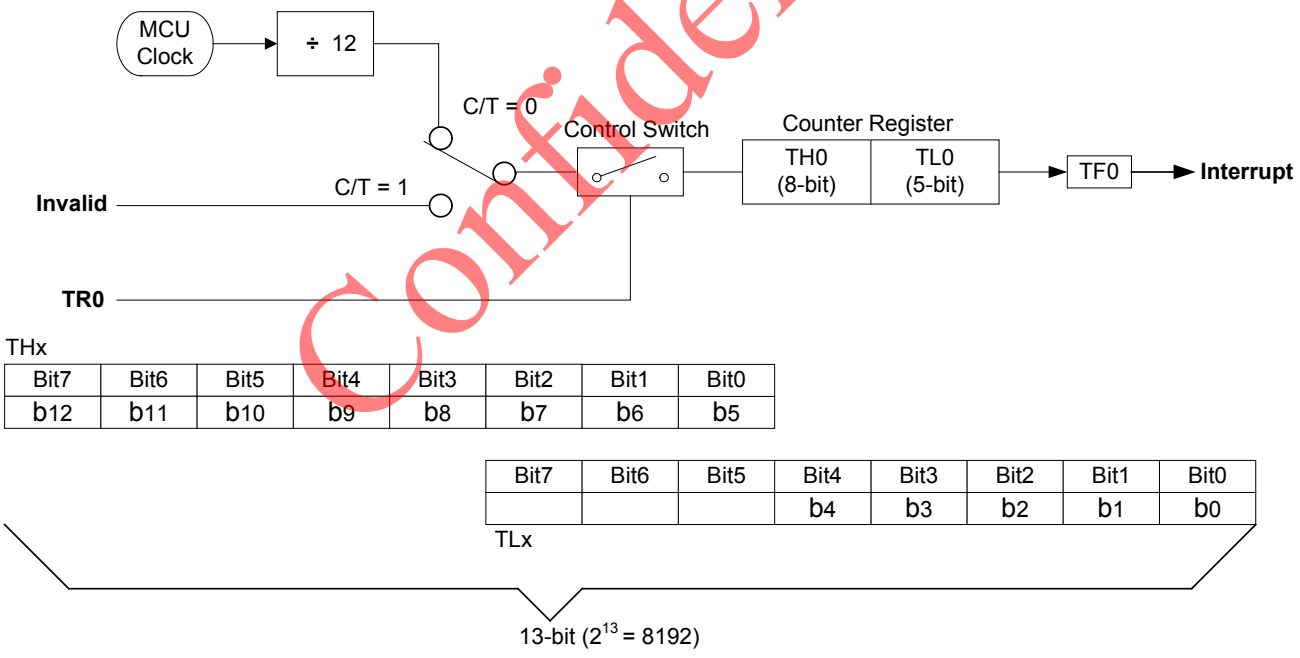
7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Bit Number	Bit Mnemonic	Description
7	TF1	Timer 1 Overflow Flag. When the Timer overflows, TF1 is set (TF1 = 1). When CPU is jumped to the Interrupt Service Routine of Timer 1, TF1 is auto-cleared (TF1 = 0).

Bit Number	Bit Mnemonic	Description
6	TR1	Timer 1 Enable bit. If TR1 is set (TR1 = 1), Timer 1 is in use; If TR1 is disabled (TR1 = 0), Timer 1 stopped.
5	TF0	Timer 0 Overflow Flag. When the Timer/Counter overflows, TF0 is set (TF0 = 1). When the CPU is jumped to the Interrupt Service Routine of Timer 0, TF0 is auto-cleared (TF0 = 0).
4	TR0	Timer 0 Enable bit. If TR0 is set (TR0 = 1), Timer 0 is in use; If TR0 is disabled (TR0 = 0), Timer 0 stopped.
3	IE1	External Interrupt INT1 Display Flag. When INT1 interrupt occurs, IE1 = 1; When interrupt finished, IE1 = 0.
2	IT1	External Interrupt INT1 interrupt signal selection. If IT1 = 1, it is negative trigger input; If IT1 = 0, it is low level input.
1	IE0	External Interrupt INT0 Display Flag, When INT0 interrupt occurs, IE0 = 1; When interrupt finished, IE0 = 0.
0	IT0	External Interrupt INT0 interrupt signal selection. If IT0 = 1, it is negative trigger input; IT0 = 0, it is low level input.

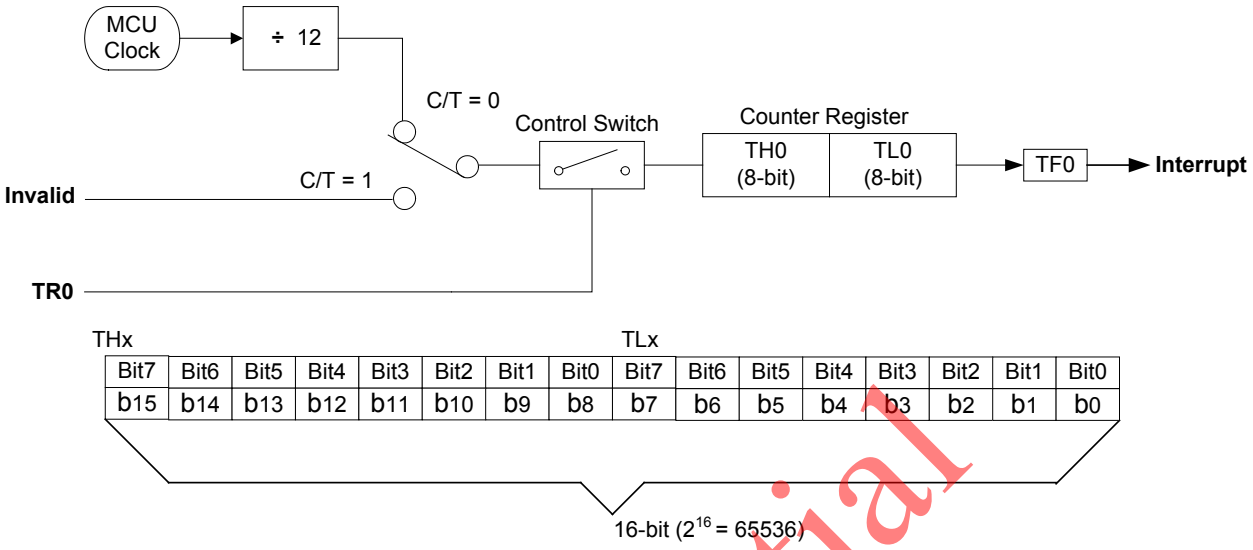
Note: See section 6.4 for more information on Baud rate generator of Timer/Counter 1.

Mode 0:



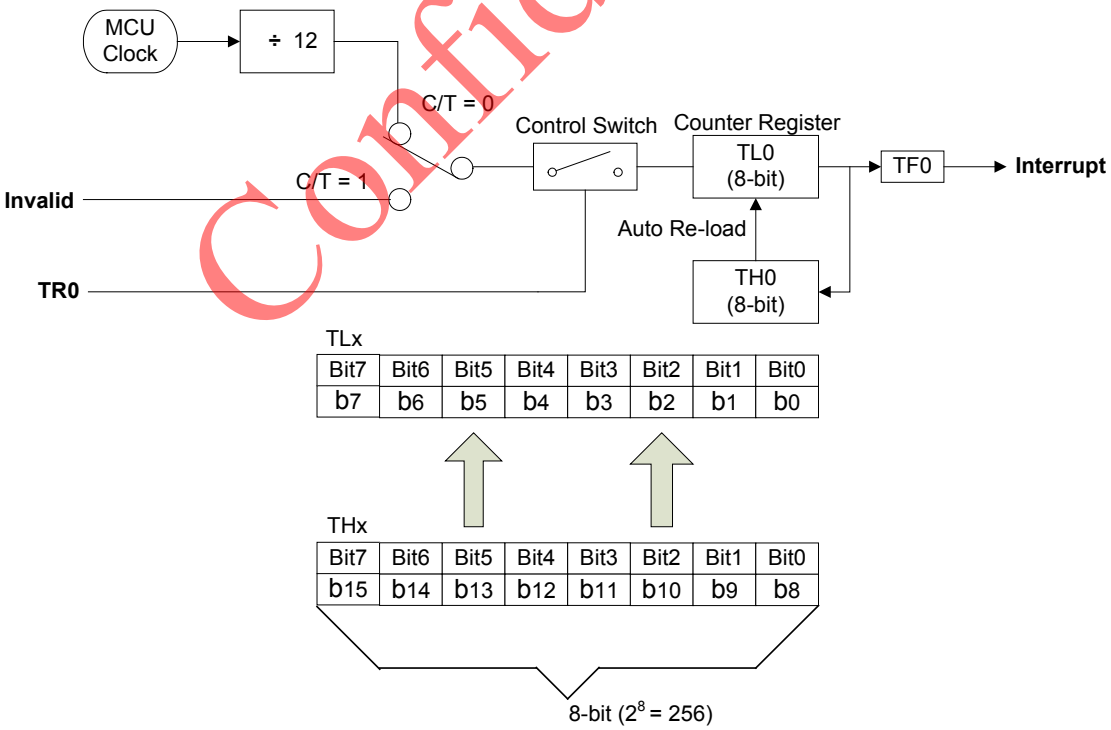
Mode 0 operation is the same for Timer 0 and Timer 1. In this mode, the timer register is configured as a 13-bit Up Timer, which is consists of the Special Function Register THx and TLx. As the count of the 13 bits is all 1s, if the register incremented 1 then count of the 13 bits is all 0s and meantime if the Timer Interrupt is enabled, an Timer overflow interrupt will occur and Overflow Flag is set (TFx = 1, and TFx locates in TCON of the Special Function Register).

Mode 1:



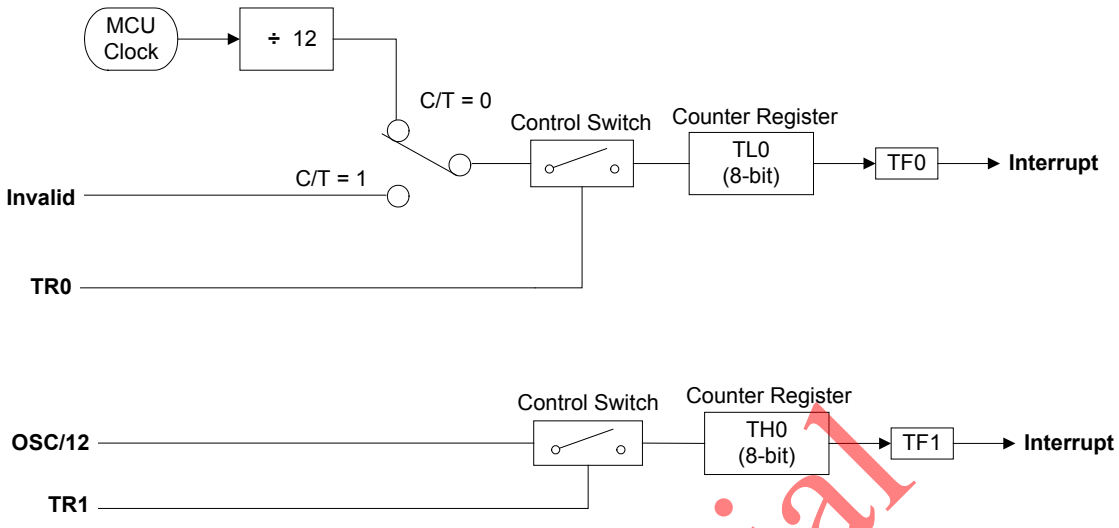
Mode 1 operation is the same as Mode 0 for Timer 0 and Timer 1, except that the Timer Register which consists of THx and TLx is configured as a 16-bit Up Timer.

Mode 2:



Mode 2 operation is the same for Timer 0 and Timer 1 to configure two 8-bit auto-reload Timers (Timer0 & Timer1). The counter value is stored in TLx Register. Overflow from TLx not only sets TFx = 1, but also auto-reloads contents of THx to TLx, and retains count.

Mode 3:

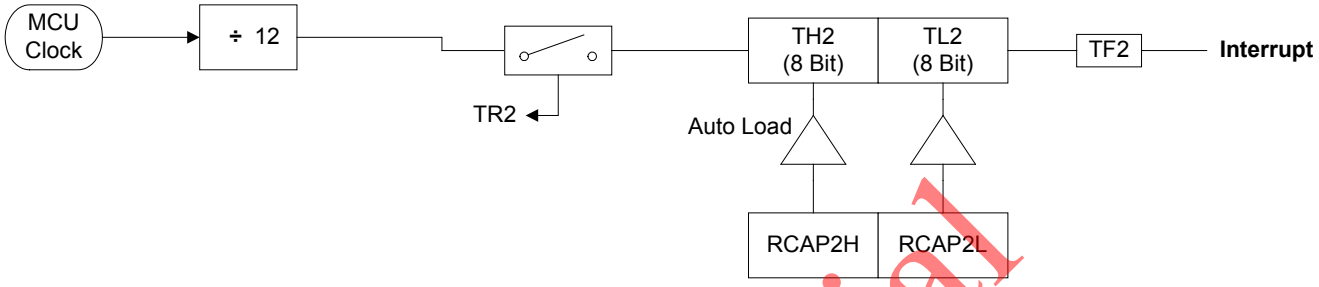


Mode 3 operation is rarely different for Timer 0 and Timer 1, as described below.
In Mode 3, TL0 is an 8-bit Timer, while TH0 is an 8-bit Counter controlled by TR1. In the meantime, be aware of the Overflow Flag of Timer 1 borrowed by TH0, and the corresponding Interrupt Service Routine address is 001BH.
In Mode 3, Timer 1 stopped and retained count.

5.6.2 Timer 2

Timer 2 16-bit Auto-Reload Mode

In Auto-Reload Mode, Timer 2 registers (TH2 and TL2) can be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, with the structure illustrated below.



T2CON (8052 Timer 2 Control Register) Address: C8H

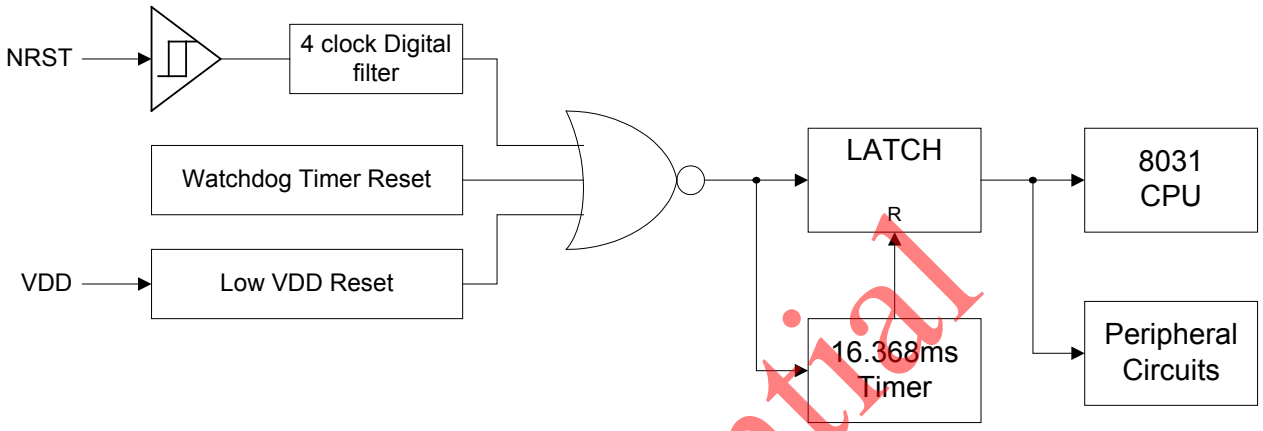
7	6	5	4	3	2	1	0
TF2	-	-	-	-	TR2	-	-

Bit Number	Bit Mnemonic	Description
7	TF2	Timer 2 Overflow Flag. When Timer 2 interrupts, TF2 is set (TF2 = 1); TF2 will not be cleared even Timer 2 interrupt terminated. It must be cleared by software (setting TF2 = 0).
6-3	Reserved	-
2	TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer. TR2 = 0 stopped the timer.
1-0	Reserved	-

When Timer 2 is turned on, Timer 2 starts the event counting. Then Timer 2 will auto reload the current value of RCAP2H and RCAP2L registers into TH2 and TL2 registers, respectively. However, the interrupt of Timer 2 will not affect the event counting. When Timer 2 counter overflows, an interrupt of Timer 2 will occur if TF2 = 1.

5.7 Reset

The WT51F516 has five reset generation sources: Power On Reset (POR), Low Voltage Reset (LVR), External NRST pin reset flag, Watchdog Reset, and ISP/ICE Command Reset. During Reset, almost all registers are reset to their initial values.



Power-on Reset (POR)

The Power-on Reset occurs when the VDD supply voltage is below the Power-on Reset voltage threshold (refer to DC Characteristics sections for more details).

Low Voltage Reset (LVR)

A reset occurs when the VDD voltage is below the operating voltage threshold.

External NRST pin reset

A reset occurs when the voltage of the external reset pin (NRST) is below its VIL (refer to DC characteristics sections for more details).

Watchdog Timer Reset)

A reset occurs when the Watchdog Timer times out.

ISP/ICE Command Reset

An ISP/ICE reset occurs when the reset command is transmitted.

Reset status

When above condition occurred, all Special Function Registers are set to their initial values. SFR contents are described in the following text. XFR contents will be discussed in next section.

The initial value of Special Function Register after Reset (as shown below):

SFR	Initial Value	SFR	Initial Value
P0	11111111b	P2	11111111b
SP	00000111b	IE	00000000b
DPL0	00000000b	P3	11111111b
DPH0	00000000b	IP	xx000000b
DPL1	00000000b	T2CON	00000000b
DPH1	00000000b	T2MOD	xxxxxx00b
DPS	00000000b	RCAP2L	00000000b
PCON	00000000b	RCAP2H	00000000b
TCON	00000000b	TL2	00000000b
TMOD	00000000b	TH2	00000000b
TL0	00000000b	PSW	00000000b
TL1	00000000b	SCON1	00000000b
TH0	00000000b	SBUF1	00000000b
TH1	00000000b	SBRG1H	00000000b
P1	11111111b	SBRG1L	00000000b
SCON0	00000000b	ACC	00000000b
SBUF0	00000000b	B	00000000b
SBRG0H	00000000b	XICON	00000000b
SBRG0L	00000000b		

6. Enhanced Function

6.1 External Special Function Register (XFR)

External Special Function Register (XFR) locates from 0x00 to 0xFF, must be acceded by the execution of MOVX instruction.

External Special Function Register table:

External memory address	Description
0000H ~ 000FH	System Register, Low Voltage Detection and Watchdog Reset Register
0010H ~ 001BH	General-purpose I/O port Register
001CH ~ 001FH	Complex Function Register
0020H ~ 0029H	Wakeup Source Setting Register
002AH ~ 002CH	Internal Oscillator Adjustment Register
0030H ~ 0035H	Interrupt Enable Register
003AH ~ 003BH	External Interrupt Request Register (IRQ)
0050H ~ 005DH	Pulse Width Modulation Register (PWM)
0060H ~ 0063H	Infrared Receiver Register (IR)
0070H ~ 0076H	Consumer Electronics Control Register (CEC)
0080H ~ 0083H	Enhanced Timer/Counter Register
00A0H ~ 00ABH	I²C Serial Port Interface Register
0038H.00B0H ~ 00BFH	Real Time Clock Module Register (RTC)
00C0H ~ 00CBH	SPI Serial Port Interface Register
00D0H ~ 00D7H	10-bit Analog/Digital Converter Register
00D9H	Comparator Register
00E0H ~ 00E8H	Simulated E²PROM Register

When the Reset status which is mentioned in section 5.7 occurred, the default value of external function register after reset is listed below:

Register Name	Address	Reset Default (Hex)	Index Section
Reserved	-	-	-
SYS System Control Register 0	0x01	82	6.7
SYS System Control Register 1	0x02	20	6.7
SYS System Control Register 2	0x03	00	6.7
SYS System Control Register 3	0x04	00	6.7
Watchdog Timer Control Register 0	0x08	00	6.9
Watchdog Timer Control Register 1	0x09	00	6.9
Watchdog Timer Control Register 2	0x0A	00	6.9
Low Voltage Detection Control Register	0x0B	80	6.18
SYS System Control Register 4	0x0F	20	6.7
General-purpose I/O Port A Output Enable Control Register	0x10	00	6.2
General-purpose I/O Port B Output Enable Control Register	0x11	00	6.2
General-purpose I/O Port C Output Enable Control Register	0x12	00	6.2
General-purpose I/O Port A Data Register	0x13	00	6.2
General-purpose I/O Port B Data Register	0x14	00	6.2
General-purpose I/O Port C Data Register	0x15	00	6.2

Register Name	Address	Reset Default (Hex)	Index Section
General-purpose I/O Port A Enable Internal Pull-up Register	0x16	FF	6.2
General-purpose I/O Port B Enable Internal Pull-up Register	0x17	FF	6.2
General-purpose I/O Port C Enable Internal Pull-up Register	0x18	FF	6.2
General-purpose I/O Port A Output Type Control Register	0x19	FF	6.2
General-purpose I/O Port B Output Type Control Register	0x1A	FF	6.2
General-purpose I/O Port C Output Type Control Register	0x1B	FF	6.2
Complex Function Setting Register 1	0x1C	00	6.3
Complex Function Setting Register 2	0x1D	00	6.3
Complex Function Setting Register 3	0x1F	00	6.3
SYS Wakeup Control Register 0	0x20	00	6.7
SYS Wakeup Control Register 1	0x21	00	6.7
SYS Wakeup Control Register 2	0x22	00	6.7
SYS Wakeup Control Register 3	0x23	00	6.7
SYS Wakeup Trigger Register 0	0x24	00	6.7
SYS Wakeup Trigger Register 1	0x25	00	6.7
SYS Wakeup Trigger Register 2	0x26	00	6.7
SYS Wakeup Trigger Register 3	0x27	00	6.7
SYS Trigger Clear Control Register	0x28	00	6.7
SYS Enhanced Timer/Counter Wakeup Control Register	0x29	00	6.7
Internal Oscillator Counter Data High Bytes Register	0x2A	00	6.8
Internal Oscillator Counter Data Low Bytes Register	0x2B	00	6.8
Internal Oscillator Calibration Control Register	0x2C	40	6.8
8052 External Interrupt 0 Control Register 0	0x30	00	6.3
8052 External Interrupt 0 Control Register 1	0x31	00	6.3
8052 External Interrupt 1 Control Register 0	0x32	00	6.3
8052 External Interrupt 1 Control Register 1	0x33	00	6.3
8052 External Interrupt Flag Register 0	0x34	00	6.3
8052 External Interrupt Flag Register 1	0x35	00	6.3
RTC Control Register 0	0x38	00	6.11
External Interrupt Request (IRQ) Control High Bytes Register	0x3A	00	6.5
External Interrupt Request (IRQ) Control Low Bytes Register	0x3B	00	6.5
PWM Control Register 0	0x50	00	6.6
PWM Control Register 1	0x51	00	6.6
PWM Clock Source Control Register 0	0x52	00	6.6
PWM Clock Source Control Register 1	0x53	00	6.6
PWM Clock Source Control Register 2	0x54	00	6.6
PWM Clock Source Control Register 3	0x55	00	6.6
PWM Duty Cycle Low Bytes Control Register 0	0x56	80	6.6
PWM Duty Cycle High Bytes Control Register 0	0x57	02	6.6
PWM Duty Cycle Low Bytes Control Register 1	0x58	80	6.6
PWM Duty Cycle High Bytes Control Register 1	0x59	02	6.6
PWM Duty Cycle Low Bytes Control Register 2	0x5A	80	6.6

Register Name	Address	Reset Default (Hex)	Index Section
PWM Duty Cycle High Bytes Control Register 2	0x5B	02	6.6
PWM Duty Cycle Low Bytes Control Register 3	0x5C	80	6.6
PWM Duty Cycle High Bytes Control Register 3	0x5D	02	6.6
Infrared Control Register	0x60	00	6.12
Infrared Interrupt Register	0x61	04	6.12
Infrared Counter Register	0x62	00	6.12
Infrared Digital Filter Register	0x63	00	6.12
CEC Control Register	0x70	00	6.10
CEC Initiator Register	0x71	10	6.10
CEC Follower Register	0x72	00	6.10
CEC Interrupt Control Register	0x73	00	6.10
CEC Clear Interrupt Register	0x74	00	6.10
CEC Transmit Buffer Register	0x75	FF	6.10
CEC Receive Buffer Register	0x76	00	6.10
Enhanced Timer/Counter Control Register 1	0x80	00	6.14
Enhanced Timer/Counter Control Register 2	0x81	00	6.14
Enhanced Timer/Counter Data Buffer High Bytes Register	0x82	00	6.14
Enhanced Timer/Counter Data Buffer Low Bytes Register	0x83	00	6.14
Slave I²C Control Register	0xA0	00	6.13
Slave I²C Interrupt Register	0xA1	00	6.13
Slave I²C Flag Clear Register	0xA2	00	6.13
Slave I²C Flag Register	0xA3	00	6.13
Slave I²C Address Register	0xA4	00	6.13
Slave I²C Index Clear Control Register	0xA8	00	6.13
Slave I²C TX FIFO Control Register	0xA9	80	6.13
Slave I²C RX FIFO Control Register	0xAA	00	6.13
Slave I²C Transmit Receive Buffer Data Register	0xAB	FF	6.13
RTC Second Control Register	0xB0	00	6.11
RTC Minute Control Register	0xB1	00	6.11
RTC Hour Control Register	0xB2	00	6.11
RTC Date Control Register	0xB3	01	6.11
RTC Week Control Register	0xB4	00	6.11
RTC Month Control Register	0xB5	01	6.11
RTC Year Control Register	0xB6	00	6.11
RTC Backup Control Register 1	0xB8	00	6.11
RTC Backup Control Register 2	0xB9	00	6.11
RTC Backup Control Register 3	0xBA	00	6.11
RTC Backup Control Register 4	0xBB	00	6.11
RTC Control Register 1	0xBC	00	6.11
RTC Control Register 2	0xBD	00	6.11
RTC Control Register 3	0xBE	81	6.11
RTC Control Register 4	0xBF	62	6.11

Register Name	Address	Reset Default (Hex)	Index Section
SPI Control Register 1	0xC0	00	6.15
SPI Interrupt Control Register	0xC1	00	6.15
SPI Interrupt Clear Register	0xC2	00	6.15
SPI Flag Register	0xC3	00	6.15
SPI Bit Rate Setting Register	0xC4	00	6.15
SPI FIFO Control Register	0xC8	00	6.15
SPI FIFO Transmit Status Register	0xC9	80	6.15
SPI FIFO Receive Status Register	0xCA	00	6.15
SPI Transmit Receive Buffer Register	0xCB	FF	6.15
ADC Control Register	0xD0	80	6.16
ADC Converted Data High Bytes Register	0xD1	00	6.16
ADC Voltage Compare Wakeup Data High Bytes Register	0xD2	80	6.16
ADC Channel Control Register	0xD3	00	6.16
ADC Converted Data Low Bytes Register	0xD4	00	6.16
ADC Voltage Compare Wakeup Data Low Bytes Register	0xD5	00	6.16
ADC Temperature Sensor Control Register	0xD6	00	6.16
ADC Setting Control Register	0xD7	04	6.16
Temperature Sensor Setting Control Register	0xD8	80	6.19
Comparator Control Register	0xD9	C0	6.17
E²PROM Enable Register 1	0xE0	00	6.20
E²PROM Enable Register 2	0xE1	00	6.20
E²PROM Address Low Bytes Register	0xE2	FF	6.20
E²PROM Address High Bytes Register	0xE3	0F	6.20
E²PROM Control Register	0xE4	08	6.20
E²PROM Data Register	0xE8	00	6.20

6.2 I/O Port

6.2.1 Features

- 24 programmable I/O, contains: GPIOA[7:0], GPIOB[7:0], and GPIOC[7:0]
- Some I/O with special functions (such as ADC, PWM exc.), can be configured by Special Function Register

6.2.2 Register

WT51F516 I/O related registers are classified into four categories:

- GPIOx_OE: Control Output/Input Register, configured to set I/O as output or input. If the corresponding bit GPIOx_OE = 1, it is an output port with 4mA driving ability
- GPIOx_D: Data Register, reading I/O data or setting output of I/O
- GPIOx_PHN: Internal Pull-up resistor Enable Register. When I/O is configured as Input port (by GPIOx_OE), this register is allowed to set if I/O is with pull-up resistor. If the corresponding GPIOx_PHN bit = 0, the I/O is with internal pull-up resistor
- GPIOx_TYP: Output mode setting Register, is configured to set I/O as Push-pull or Open drain type

General-purpose I/O Port A Output Enable Control Register GPIOA_OE (XFR: 0x10) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_OE[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOA_OE[7:0]	General-purpose I/O Port A Output/Input setting 1: Output 0: Input (default)

General-purpose I/O Port B Output Enable Control Register GPIOB_OE (XFR: 0x11) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_OE[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOB_OE[7:0]	General-purpose I/O Port B Output/Input setting 1: Output 0: Input (default)

General-purpose I/O Port C Output Enable Control Register GPIOC_OE (XFR: 0x12) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOC_OE[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOC_OE[7:0]	General-purpose I/O Port C Output/Input setting 1: Output 0: Input (default)

General-purpose I/O Port A Data Register GPIOA_D (XFR: 0x13) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_D[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOA_D[7:0]	General-purpose I/O Port A Output/Input Data

General-purpose I/O Port B Data Register GPIOB_D (XFR: 0x14) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_D[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOB_D[7:0]	General-purpose I/O Port B Output/Input Data

General-purpose I/O Port C Data Register GPIOC_D (XFR: 0x15) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOC_D[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOC_D[7:0]	General-purpose I/O Port C Output/Input Data

General-purpose I/O Port A Enable Internal Pull-up Register GPIOA_PHN (XFR: 0x16) **Reset Value: FFh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_PHN[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOA_PHN[7:0]	Enable General-purpose I/O Port A Pull-up Resistor setting 1: Disable Pull-up Resistor (default) 0: Enable Pull-up Resistor

General-purpose I/O Port B Enable Internal Pull-up Register GPIOB_PHN (XFR: 0x17) Reset Value: FFh

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_PHN[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOB_PHN[7:0]	Enable General-purpose I/O Port B Pull-up Resistor setting 1: Disable Pull-up Resistor (default) 0: Enable Pull-up Resistor

General-purpose I/O Port C Enable Internal Pull-up Register GPIOC_PHN (XFR: 0x18) Reset Value: FFh

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOC_PHN[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOC_PHN[7:0]	Enable General-purpose I/O Port C Pull-up Resistor setting 1: Disable Pull-up Resistor (default) 0: Enable Pull-up Resistor

General-purpose I/O Port A Output Type Control Register GPIOA_TYP (XFR: 0x19) Reset Value: FFh

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_TYP[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOA_TYP[7:0]	General-purpose I/O Port A output type setting 1: Push-pull output type (default) 0: Open-drain output type

General-purpose I/O Port B Output Type Control Register GPIOB_TYP (XFR: 0x1A) Reset Value: FFh

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_TYP[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOB_TYP[7:0]	General-purpose I/O Port B output type setting 1: Push-pull output type (default) 0: Open-drain output type

General-purpose I/O Port C Output Type Control Register GPIOC_TYP (XFR: 0x1B) **Reset Value: FFh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOC_TYP[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOC_TYP[7:0]	General-purpose I/O Port C output type setting 1: Push-pull output type (default) 0: Open-drain output type

6.2.3 Port Sharing

This is use to set I/O functions, such as SPI, I²C, PWM, ADC, etc.

Complex Function Setting Register 1 GPIO_FUN1 (XFR: 0x1C) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	EN_SIIC_IO	EN_SPI_IO	EN_CEC_IO	EN_UART0_IO	EN_PWM_IO[3:0]			

Bit Number	Bit Mnemonic	Description
7	EN_SIIC_IO	Set GPIO Complex Function 1: Enable I²C SDA/SCL pin, and was forced to set GPIO as I²C SDA/SCL pin instead of GPIO function 0: GPIO (default)
6	EN_SPI_IO	Set GPIO Complex Function 1: Enable SPI MISO/MOSI/SCK pin, and was forced to set GPIO as SPI MISO/MOSI/SCK pin instead of GPIO function 0: GPIO (default)
5	EN_CEC_IO	Set GPIO Complex Function 1: Enable CEC pin, and was forced to set GPIO as CEC pin instead of GPIO function 0: GPIO (default)
4	EN_UART0_IO	Set GPIO Complex Function 1: Enable UART0 pin, and was forced to set GPIO as UART0 pin instead of GPIO function 0: GPIO (default)
3-0	EN_PWM_IO[3:0]	Set GPIO Complex Function 1: Enable PWM pin, and was forced to set GPIO as PWM pin instead of GPIO function 0: GPIO (default)

Complex Function Setting Register 2 GPIO_FUN2 (XFR: 0x1D) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	EN_AD_IO[7:0]							

Bit Number	Bit Mnemonic	Description
7	EN_AD_IO[7:0]	Set GPIO Complex Function 1: Enable ADC7 pin, and was forced to set GPIO as ADC7 pin instead of GPIO function 0: GPIO (default)
6		Set GPIO Complex Function 1: Enable ADC6 pin, and was forced to set GPIO as ADC6 pin instead of GPIO function 0: GPIO (default)
5		Set GPIO Complex Function 1: Enable ADC5 pin and was forced to set GPIO as ADC5 pin instead of GPIO function 0: GPIO (default)
4		Set GPIO Complex Function 1: Enable ADC4 pin and was forced to set GPIO as ADC4 pin instead of GPIO function 0: GPIO (default)
3		Set GPIO Complex Function 1: Enable ADC3 pin and was forced to set GPIO as ADC3 pin instead of GPIO function 0: GPIO (default)
2		Set GPIO Complex Function 1: Enable ADC2 pin and was forced to set GPIO as ADC2 pin instead of GPIO function 0: GPIO (default)
1		Set GPIO Complex Function 1: Enable ADC1 pin and was forced to set GPIO as ADC1 pin instead of GPIO function 0: GPIO (default)
0		Set GPIO Complex Function 1: Enable ADC0 pin and was forced to set GPIO as ADC0 pin instead of GPIO function 0: GPIO (default)

Complex Function Setting Register 3 GPIO_FUN3 (XFR: 0x1F) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	–	–	R/W	R/W	R/W	R/W
Name	EN_ACOMP_IO	EN_UART1_IO	Reserved		EN_P0_IO[3:0]			

Bit Number	Bit Mnemonic	Description
7	EN_ACOMP_IO	Set GPIO Complex Function 1: Enable ACOMP pin and was forced to set GPIO as ACOMP pin instead of GPIO function 0: GPIO (default)
6	EN_UART1_IO	Set GPIO Complex Function 1: EnableUART1 pin and was forced to set GPIO as UART1 pin instead of GPIO function 0: GPIO (default)
5-4	Reserved	-
3-0	EN_P0_IO[3:0]	Set GPIO Complex Function 1: Enable 8051 P0[x] pin and was forced to set GPIO as 8051 P0[x] pin instead of GPIO function 0: GPIO (default)

-: unimplemented.

Note:

(a) EN_P0_IO[3:0]: Enable P0[3:0] IO PAD, and IO type depends on GPIOx_TYP[x] setting

(b) UG320/32A GPIOC1 pin, when PIN#2 (GPIOC1/XTALO) is configured as GPIO, PIN#1(XTALI) must be connected to ground.

(c) Some GPIO ports have no wire-bondings at 20-pin or 16-pin package type. These pins must enable internal pull high for power saving.

ADC Complex Function Setting Table:

ADC	Register Setting	Shared with GPIO
ADC7	EN_AD_IO[7]	GPIOB7
ADC6	EN_AD_IO[6]	GPIOB6
ADC5	EN_AD_IO[5]	GPIOB5
ADC4	EN_AD_IO[4]	GPIOB4
ADC3	EN_AD_IO[3]	GPIOB3
ADC2	EN_AD_IO[2]	GPIOB2
ADC1	EN_AD_IO[1]	GPIOB1
ADC0	EN_AD_IO[0]	GPIOB0

ADC VREF Complex Function Setting Table:

ADC VREF	Register Setting	Shared with GPIO
VREF	VREF_SEL[2:0]	GPIOA7

SPI Complex Function Setting Table:

SPI	Register Setting	Shared with GPIO
SCK	EN_SPI_IO	GPIOC7
MOSI	EN_SPI_IO	GPIOA5
MISO	EN_SPI_IO	GPIOC6
STB	EN_SPI_IO	GPIOA4

UART Complex Function Setting Table:

UART	Register Setting	Shared with GPIO
RXD	EN_UART0_IO	GPIOC3
TXD	EN_UART0_IO	GPIOC4
RXD1	EN_UART1_IO	GPIOC6
TXD1	EN_UART1_IO	GPIOC7

I²C Complex Function Setting Table:

I²C	Register Setting	Shared with GPIO
SDA	EN_SIIC_IO	X
SCL	EN_SIIC_IO	X

Comparator Complex Function Setting Table:

ACOM	Register Setting	Shared with GPIO
ACIN	EN_ACOMP_IO	GPIOB1
ACIP	EN_ACOMP_IO	GPIOB0
ACO	EN_ACOMP_IO	GPIOA0

PWM Complex Function Setting Table:

PWM	Register Setting	Shared with GPIO
PWM0	EN_PWM_IO[0]	GPIOC5
PWM1	EN_PWM_IO[1]	GPIOA0
PWM2	EN_PWM_IO[2]	GPIOA3
PWM3	EN_PWM_IO[3]	GPIOA4

CEC Complex Function Setting Table:

PWM	Register Setting	Shared with GPIO
CEC	EN_CEC_IO	GPIOA2

6.3 Interrupt

The WT51F516 provides total seven 8052 Interrupt sources: two 8052 External Interrupts (INT0, INT1), three Timer/Counter Interrupts (TF0, TF1, TF2), and two UART Interrupts (RI0/TI0, RI1/TI1).

Each of these interrupt sources has its own enable control bit, and can be individually enabled or disabled by setting or clearing the corresponding bit in the Special Function Register IE or XICON.

When an interrupt is generated, CPU will jump to interrupt vector from service routine as listed below. If multiple requests of different priority levels are received simultaneously, the request of higher priority level is serviced, and then returned to service routine through RETI instruction. If interrupt flag bit is set, CPU will enter the Interrupt processing again.

Interrupt Vector Table of 8052 & Priority Level Structure:

Interrupt sources	Vector Address	Priority Level (default)	Interrupt Enable Register
8052 external interrupt 0	03H	1	IE.0 (EX0)
Timer/Counter 0 interrupt	0BH	2	IE.1 (ET0)
8052 external interrupt 1	13H	3	IE.2 (EX1)
Timer/Counter 1 interrupt	1BH	4	IE.3 (ET1)
Serial port 0 interrupt (UART0)	23H	5	IE.4 (ES)
Timer/Counter 2 interrupt	2BH	6	IE.5 (ET2)
Serial port 1 interrupt (UART1)	33H	7	IE.6 (ES1)

Interrupt Enable Register 0

IE0 (8052 interrupt enable register, including INT0/INT1) Address: A8H **Reset Value: 0x00**

7	6	5	4	3	2	1	0
EA	ES1	ET2	ES	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	1: Enable all interrupt function 0: Disable all interrupt function
6	ES1	1: Enable UART 1 interrupt 0: Disable UART 1 interrupt
5	ET2	1: Enable Timer/Counter 2 interrupt 0: Disable Timer/Counter 2 interrupt
4	ES	1: Enable UART 0 interrupt 0: Disable UART 0 interrupt
3	ET1	1: Enable Timer/Counter 1 interrupt 0: Disable Timer/Counter 1 interrupt
2	EX1	1: Enable 8052 external interrupt 1 interrupt 0: Disable 8052 external interrupt 1 interrupt
1	ET0	1: Enable Timer/Counter 0 interrupt 0: Disable Timer/Counter 0 interrupt
0	EX0	1: Enable 8052 external interrupt 0 interrupt 0: Disable 8052 external interrupt 0 interrupt

Interrupt Priority Register

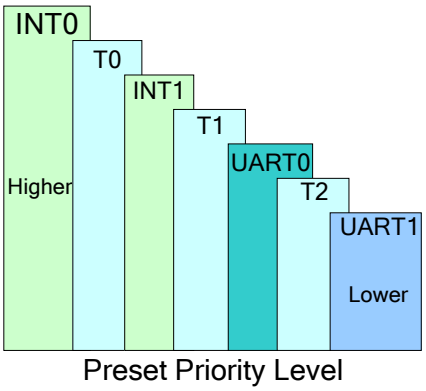
IP (8052 interrupt priority register) Address: B8H **Reset Value: 0x00**

7	6	5	4	3	2	1	0
-	PS1	PT2	PS	PT1	PX1	PT0	PX0

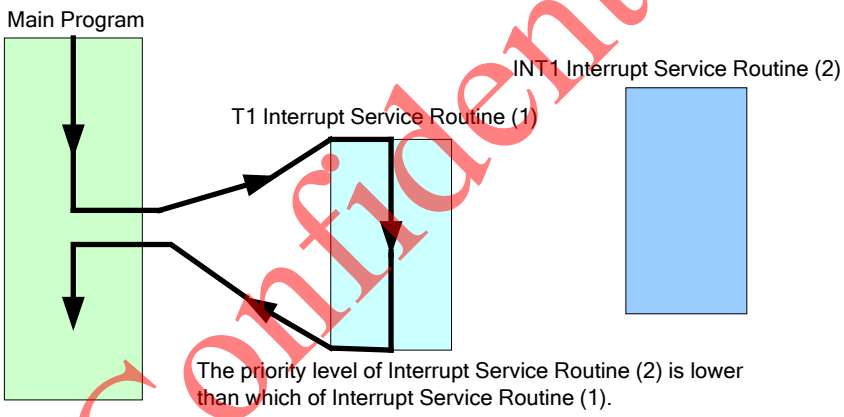
Bit Number	Bit Mnemonic	Description
7	Reserved	-
6	PS1	Define the interrupt priority of UART 1 1: has the higher priority 0: has the lower priority
5	PT2	Define the interrupt priority of Timer/Counter 2 1: has the higher priority 0: has the lower priority
4	PS	Define the interrupt priority of UART 0 1: has the higher priority 0: has the lower priority
3	PT1	Define the interrupt priority of Timer/Counter 1 1: has the higher priority 0: has the lower priority
2	PX1	Define the interrupt priority of External Interrupt 1 1: has the higher priority 0: has the lower priority
1	PT0	Define the interrupt priority of Timer/Counter 0 1: has the higher priority 0: has the lower priority
0	PX0	Define the interrupt priority of External Interrupt 0 1: has the higher priority 0: has the lower priority

-: unimplemented.

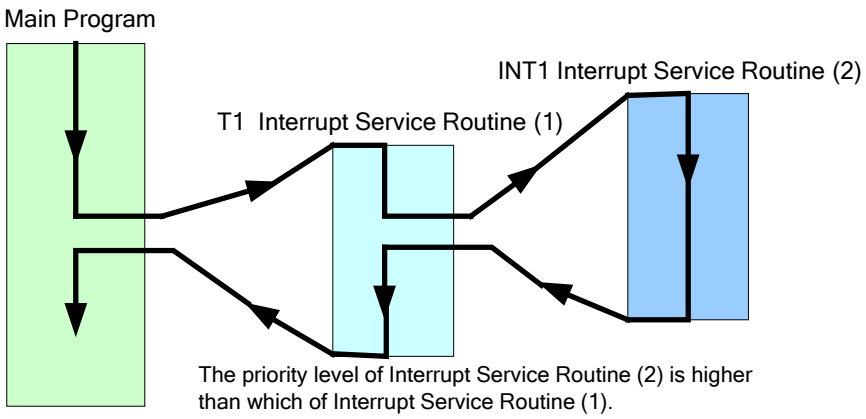
As illustrated below, if the priority level in Interrupt Priority Register (IP) is not set, the priority level of interrupt will be: **INT0 > T0 > INT1 > T1 > UART0 > T2 > UART1**



If the higher priority is assigned to any one of the interrupts, such as set PT1 = 1, then the priority level will be: **T1 > INT0 > T0 > INT1 > UART0 > T2 > UART1**



If PT1 = 1 and PX1 = 1, then the priority level will be: **INT1 > T1 > INT0 > T0 > UART0 > T2 > UART1**, and so on. The figure below illustrated the executing procedures under different priority levels.

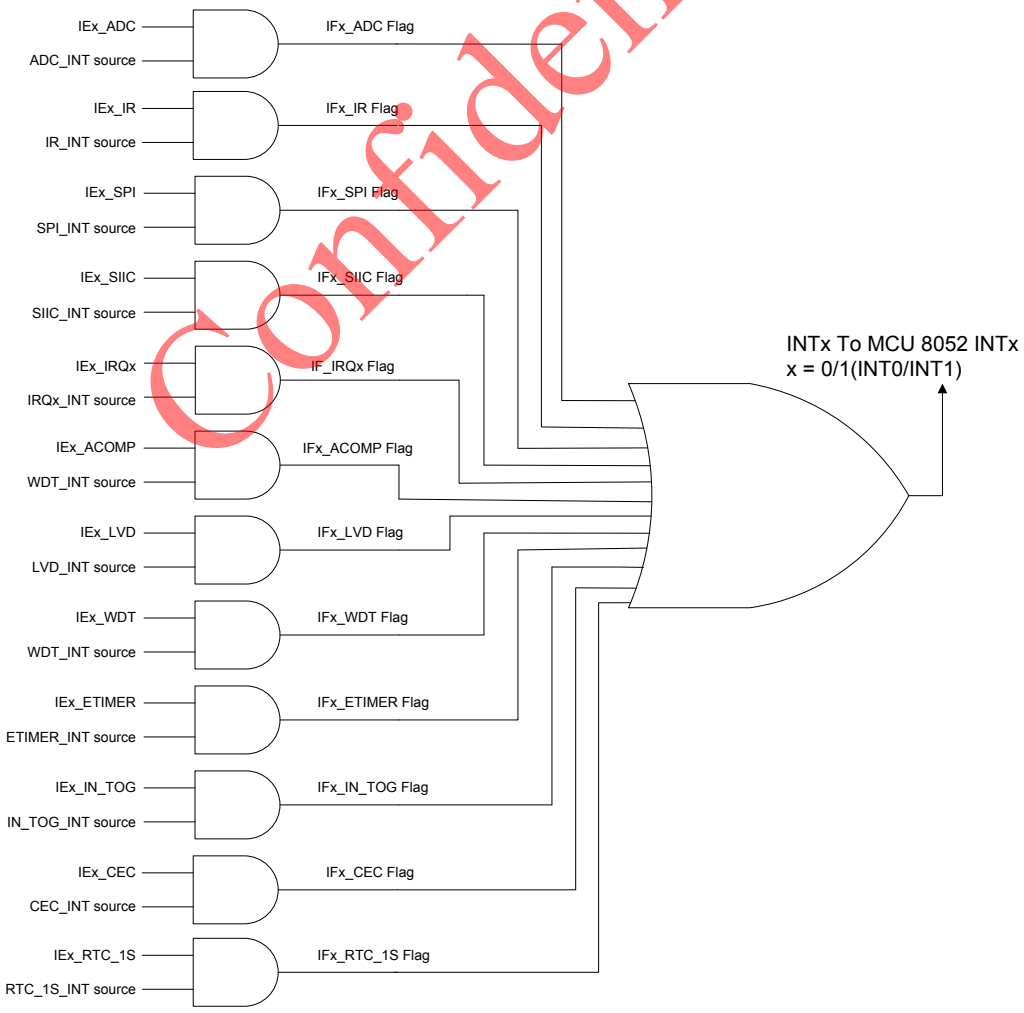


6.3.1 8052 External Interrupt 0/1

The WT51F516 supports twelve peripheral interrupt sources which are derived from 8052 external interrupt 0/1, as described below.:

1. SPI interrupt
2. I²C interrupt
3. Comparator (ACOMP) interrupt
4. Low Voltage Detection (LVD) interrupt
5. Watch Timer interrupt
6. Enhanced Timer/Counter interrupt
7. Enhanced general-purpose I/O port input triggered interrupt
8. IR interrupt
9. CEC interrupt
10. IRQ External Interrupt
11. ADC interrupt
12. RTC 1S interrupt

The figure below shows the interrupt sources of 8052 external interrupt 0/1:



8052 External Interrupt 0 Control Register 0 IE0_CTL0 (XFR: 0x30) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W
Name	IE0_ETM	IE0_IN_TOG	IE0_LVD	IE0_WDT	IE0_ACOMP	Reserved	IE0_SPI	IE0_SIIC

Bit Number	Bit Mnemonic	Description
7	IE0_ETM	1: Enable Enhanced Timer Interrupt generated by INT0 0: Disable Enhanced Timer Interrupt generated by INT0
6	IE0_IN_TOG	1: Enable All-Input Toggle Interrupt generated by INT0 0: Disable All-Input Toggle Interrupt generated by INT0
5	IE0_LVD	1: Enable LVD Interrupt generated by INT0 0: Disable LVD Interrupt generated by INT0
4	IE0_WDT	1: Enable Watch Timer Interrupt generated by INT0 0: Disable Watch Timer Interrupt generated by INT0
3	IE0_ACOMP	1: Enable ACOMP Interrupt generated by INT0 0: Disable ACOMP Interrupt generated by INT0
2	Reserved	-
1	IE0_SPI	1: Enable SPI Interrupt generated by INT0 0: Disable SPI Interrupt generated by INT0
0	IE0_SIIC	1: Enable SI²C Interrupt generated by INT0 0: Disable SI²C Interrupt generated by INT0

-: unimplemented.

8052 External Interrupt 0 Control Register 1 IE0_CTL1 (XFR: 0x31) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IE0_IRQ[3:0]				IE0_RTC_1S	IE0_KADC	IE0_IR	IE0_CEC

Bit Number	Bit Mnemonic	Description
7-4	IE0_IRQ[3:0]	1: Enable IRQ[3:0] Interrupt generated by INT0 0: Disable IRQ[3:0] Interrupt generated by INT0
3	IE0_RTC_1S	1: Enable RTC1S Interrupt generated by INT0 0: Disable RTC1S Interrupt generated by INT0
2	IE0_KADC	1: Enable ADC Interrupt generated by INT0 0: Disable ADC Interrupt generated by INT0
1	IE0_IR	1: Enable IR Interrupt generated by INT0 0: Disable IR Interrupt generated by INT0
0	IE0_CEC	1: Enable CEC Interrupt generated by INT0 0: Disable CEC Interrupt generated by INT0

8052 External Interrupt 1 Control Register 0 IE1_CTL0 (XFR: 0x32) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W
Name	IE1_ETM	IE1_IN_TOG	IE1_LVD	IE1_WDT	IE1_ACOMP	Reserved	IE1_SPI	IE1_SIIC

Bit Number	Bit Mnemonic	Description
7	IE1_ETM	1: Enable Enhanced Timer Interrupt generated by INT1 0: Disable Enhanced Timer Interrupt generated by INT1
6	IE1_IN_TOG	1: Enable All-Input Toggle Interrupt generated by INT1 0: Disable All-Input Toggle Interrupt generated by INT1
5	IE1_LVD	1: Enable LVD Interrupt generated by INT1 0: Disable LVD Interrupt generated by INT1
4	IE1_WDT	1: Enable Watch Timer Interrupt generated by INT1 0: Disable Watch Timer Interrupt generated by INT1
3	IE1_ACOMP	1: Enable ACOMP Interrupt generated by INT1 0: Disable ACOMP Interrupt generated by INT1
2	Reserved	-
1	IE1_SPI	1: Enable SPI Interrupt generated by INT1 0: Disable SPI Interrupt generated by INT1
0	IE1_SIIC	1: Enable SI²C Interrupt generated by INT1 0: Disable SI²C Interrupt generated by INT1

-: unimplemented.

8052 External Interrupt 1 Control Register 1 IE1_CTL1 (XFR: 0x33) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IE1_IRQ[3:0]				IE1_RTC_1S	IE1_KADC	IE1_IR	IE1_CEC

Bit Number	Bit Mnemonic	Description
7-4	IE1_IRQ[3:0]	1: Enable IRQ[3:0] Interrupt generated by INT1 0: Disable IRQ[3:0] Interrupt generated by INT1
3	IE1_RTC_1S	1: Enable RTC1S Interrupt generated by INT1 0: Disable RTC1S Interrupt generated by INT1
2	IE1_KADC	1: Enable ADC Interrupt generated by INT1 0: Disable ADC Interrupt generated by INT1
1	IE1_IR	1: Enable IR Interrupt generated by INT1 0: Disable IR Interrupt generated by INT1
0	IE1_CEC	1: Enable CEC Interrupt generated by INT1 0: Disable CEC Interrupt generated by INT1

8052 External Interrupt Flag Register 0 IF_FLAG0 (XFR: 0x34) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	-	R	R
Name	IF_ETM	IF_IN_TOG	IF_LVD	IF_WDT	IF_ACOMP	Reserved	IF_SPI	IF_SIIC

Bit Number	Bit Mnemonic	Description
7	IF_ETM	1: Enhanced Timer Interrupt Event Flag be set
6	IF_IN_TOG	1: All-Input Toggle Interrupt Event Flag be set
5	IF_LVD	1: LVD Interrupt Event Flag be set
4	IF_WDT	1: Watch Timer Interrupt Event Flag be set

Bit Number	Bit Mnemonic	Description
3	IF_ACOMP	1: ACOMP Interrupt Event Flag be set
2	Reserved	-
1	IF_SPI	1: SPI Interrupt Event Flag be set
0	IF_SIIC	1: S I²C Interrupt Event Flag be set

-: unimplemented.

8052 External Interrupt Flag Register 1 IF_FLAG1 (XFR: 0x35) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	IF_IRQ[3:0]				IF_RTC_1S	IF_KADC	IF_IR	IF_CEC

Bit Number	Bit Mnemonic	Description
7-4	IF_IRQ[3:0]	1: IRQ Interrupt Event Flag be set, IRQ Interrupt Flag Clear
3	IF_RTC_1S	1: RTC 1S Toggle Interrupt Event Flag be set, RTC_1S Toggle Interrupt Flag Clear
2	IF_KADC	1: ADC Interrupt Event Flag be set, ADC Interrupt Flag Clear
1	IF_IR	1: IR Interrupt Event Flag be set, IR Interrupt Flag Clear
0	IF_CEC	1: CEC Interrupt Event Flag be set, CEC Interrupt Flag Clear

6.4 Universal Asynchronous Receiver-Transmitter (UART)

The WT51F516 contains two Universal Asynchronous Receiver-Transmitters (UART0 and UART1).

As a standard UART of 8052, the Baud rate is selected by the Serial Baud rate Generator in SFR.

On Transmit and Receive, the SFR SBUFx uses two separate registers: a transmit buffer and a receive buffer register.

Transmitting data: Writing to SBUFx register and loads these data in serial output buffer, and starts transmitting.
Receiving data: Reading SBUFx register and reading the serial receive buffer. The serial port can transmit and receive simultaneously. It is also one byte receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register to prevent data loss.

The peripheral registers of UART:

SFR Name	Address	Description
PCON	87H	8052 Power Control Register
SCON0	98H	UART 0, Control Register
SBUF0	99H	UART 0, Data Buffer
SBRG0H	9AH	Serial Baud rate Generator, high byte
SBRG0L	9BH	Serial Baud rate Generator, low byte
SCON1	D8H	UART 1, Control Register
SBUF1	D9H	UART 1, Data Buffer
SBRG1H	DAH	Serial Baud rate Generator 1, high byte
SBRG1L	DBH	Serial Baud rate Generator 1, low byte

UART0 Peripheral Registers

PCON (8052 Power Control Register) Address: 87H

7	6	5	4	3	2	1	0
SMOD	-	-	-	-	-	-	-

SMOD: UART0 dual rate bit.

-: unimplemented.

SBUF0 (8052 UART0 buffer) Address: 99H

7	6	5	4	3	2	1	0
SBUF0.7	SBUF0.6	SBUF0.5	SBUF0.4	SBUF0.3	SBUF0.2	SBUF0.1	SBUF0.0

The Serial Data Buffer of UART0. It is used to hold the bytes to be received or the bytes to be transmitted from UART0.

SBRG0H: Address: 9Ah

7	6	5	4	3	2	1	0
SBRG_EN	BRG_M[10]	BRG_M[9]	BRG_M[8]	BRG_M[7]	BRG_M[6]	BRG_M[5]	BRG_M[4]

Used to configure the Baud rate of UART0 and it must be accessed together with SBRG0L.

SBRG0L: Address: 9Bh

7	6	5	4	3	2	1	0
BRG_M[3]	BRG_M[2]	BRG_M[1]	BRG_M[0]	BRG_F[3]	BRG_F[2]	BRG_F[1]	BRG_F[0]

Used to configure the Baud rate of UART0 and it must be accessed together with SBRG0H.

SCON0 (8052 UART0 Control Register) Address: 98H

7	6	5	4	3	2	1	0
SM0_1	SM0_2	SM0_3	REN_0	TB8_0	RB8_0	TI_0	RI_0

Bit Number	Bit Mnemonic	Description
7-6	SM0_1, SM0_2	UART0 mode selection 00: Mode 0 01: Mode 1 10: Mode 2 11: Mode 3
5	SM0_3	Multi-processor Communication Enable bit In Mode 0, if SM0_3 = 0, the multi-processor communication function is disabled. In Mode 1, 2, or 3, if SM0_3 = 1, the multi-processor communication function is enabled.
4	REN_0	UART Receive Enable bit must be cleared by software. REN_0 = 1, receive starts. REN_0 = 0, receive stops.
3	TB8_0	The 9th transmit bit in Mode 2 or Mode 3, can be set or cleared by software.
2	RB8_0	In Mode 0, this bit is invalid. In Mode 1, this bit is Stop bit if SM0_3 = 0 In Mode 2 or 3, the 9th data bit that was received.
1	TI_0	Transmit Interrupt Flag. When an interrupt is complete, this bit will not be restored to “0”, and it must be cleared by software. In Mode 0, this bit is set by hardware at the end of the 8th bit, and meantime it can commence a TI_0 interrupt. In Mode 1, 2, or 3, this bit is set by hardware at the end of transmitting Stop bit, and meantime it can commence a TI_0 interrupt.
0	RI_0	Receive Interrupt Flag. When an interrupt is complete, this bit will not be restored to “0”, and it must be cleared by software. In Mode 0, this bit is set by hardware at the end of the 8th bit, and meantime it can commence a RI_0 interrupt. In Mode 1, 2, or 3, this bit is set by hardware at the end of transmitting Stop bit, and meantime it can commence a RI_0 interrupt.

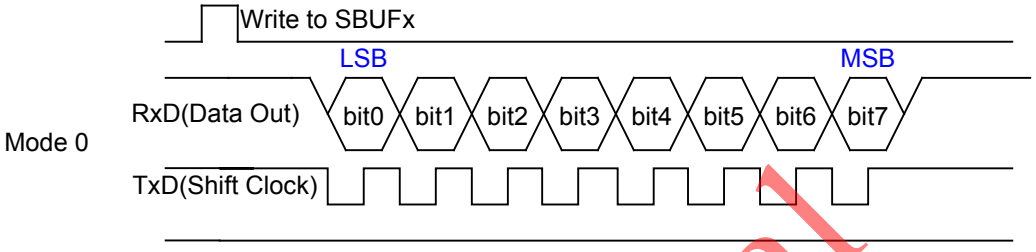
The Serial Interface 0 can operate in four modes, as described below.

SM0_1	SM0_2	Mode	Function	Baud Rate
0	0	0	Shift Register	Fosc/12
0	1	1	8-bit UART	Software programmed
1	0	2	8-bit UART	Fosc/32 or Fosc/64
1	1	3	9-bit UART	Software programmed

***Fosc = MCU clock**

Mode 0

In Mode 0, the Baud rate of Shift transmission register is fixed at 1/12 of the oscillator frequency (*fOSC*/12). At 12 MHz, the Baud rate is 1Mbps. In this mode, no matter on receive or transmit data, RxD of CPUs connects each other worked as a serial data bus and TxD connects each other worked as a Shift pulse. On Receive, TxD pin sent out the shift pulse, and the serial data was received by RxD pin; On Transmit, it is also based on the shift pulse sent by TxD pin, and sent the serial data by RxD pin.

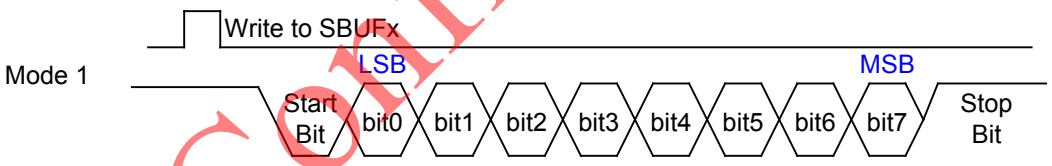


Mode 1

Mode 1 may have a variable Baud rate for serial data transmit, and the Baud rate is controlled by Timer 1. (If UART1 is supported, Timer 2 is also available for controlling the Baud rate).

In this mode, the RxD pin of WT51F516 connects to the destination TxD pin, and the Tx0 pin of WT51F516 connects to the destination RxD pin.

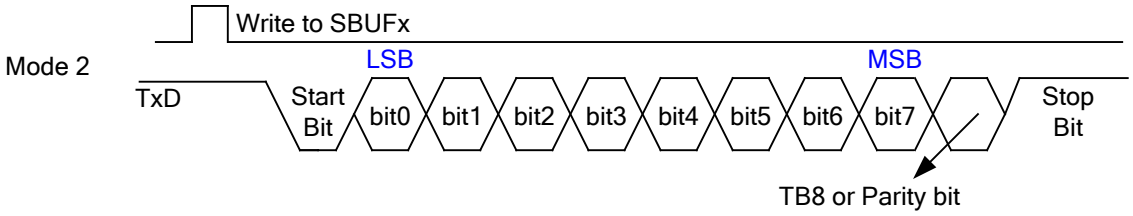
10 bits are length of transmitted or received: a Start bit, 8 data bits, and a Stop bit. The first bit is the low level start bit (0), followed by the 8 data bits (LSB first, starts from bit 0), then the high level stop bit (1) after bit 7 (MSB).



Mode 2

Mode 2 operates at *fOSC*/32 (SMOD = 1) or *fOSC*/64 (SMOD = 0) for serial data transmission. As for the wire connection, RxD pin of WT51F516 connects to destination TxD pin and TxD pin of WT51F516 connects to destination RxD pin. 11 bits are length of transmitted or received: a Start bit, 8 data bits, a Parity bit, and 1 Stop bit. The first bit is the low level start bit (0), followed by the 8 data bits (LSB first, starts from bit 0), then the Parity bit after bit 7, and finally the high level stop bit.

On Transmit, TB8_0 in SCON0 is the 9th data bit. The TB8_0 in SCON0 will transmit the 9th data bit; On Receive, the RB8_0 in SCON0 will receive the 9th data bit.



Mode 3

The Baud rate in mode 3 is variable for serial data transmission, and it is controlled by Timer 1 (If UART1 is supported, Timer 2 is allowed to control the Baud rate). The operations in Mode 3 is the same as Mode 2.

Serial Baud rate of UART0:

SBRG_EN (SBRG0H.7)	SMOD1 (PCON.7)	Baud Rate for UART0
0	0	$\frac{1}{32}\times\frac{f_{osc}}{12\times(256-TH1)}$
0	1	$\frac{1}{16}\times\frac{f_{osc}}{12\times(256-TH1)}$
1	X	$\frac{f_{osc}}{16*(BRG\_M[10:0]+\frac{BRG\_F[3:0]}{16})}$

If SBRG_EN (SBRG0H.7) = 1

$$\text{UART0 Baud rate} = \frac{f_{osc}}{16*(BRG\_M[10:0]+\frac{BRG\_F[3:0]}{16})}$$

Baud rate supporting table:

	12 MHz				
Bits/sec	**Baud Rate Register**	**BRG_M**	**BRG_F**	**Actual**	**Error**
600	1250	1250	0	600	0.0%
1200	625	625	0	1200	0.0%
2400	312.5	312	8	2400	0.0%
4800	156.25	156	4	4800	0.0%
9600	78.125	78	2	9600	0.0%
14400	52.083	52	1	14405	0.04%
19200	39.0625	39	1	19200	0.0%
38400	19.531	19	8	38461	0.16%
57600	13	13	0	57692	0.16%
115200	6.5	6	8	115384	0.16%
230400	3.25	3	4	230769	0.16%

UART1 Peripheral Register

SBUF1 (8052 UART1 buffer) Address: D9H

7	6	5	4	3	2	1	0
SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0

Serial data buffer of UART1, It is used to hold the bytes to be received or the bytes to be transmitted from UART.

SBRG1H: Address: DAh

7	6	5	4	3	2	1	0
SBRG1_EN	BRG1_M[10]	BRG1_M[9]	BRG1_M[8]	BRG1_M[7]	BRG1_M[6]	BRG1_M[5]	BRG1_M[4]

Used to configure the Baud rate of UART1 and it must be accessed together with SBRG1L.

SBRG1L: Address: DBh

7	6	5	4	3	2	1	0
BRG1_M[3]	BRG1_M[2]	BRG1_M[1]	BRG1_M[0]	BRG1_F[3]	BRG1_F[2]	BRG1_F[1]	BRG1_F[0]

Used to configure the Baud rate of UART1 and it must be accessed together with SBRG1H.

SCON1 (8052 UART1 Control Register) Address: D8H

7	6	5	4	3	2	1	0
SM1_1	SM1_2	SM1_3	REN_1	TB8_1	RB8_1	TI_1	RI_1

UART 1 Control Register

Bit Number	Bit Mnemonic	Description
7-6	SM1_1, SM1_2	UART1 mode selection 00: Mode 0 01: Mode 1 10: Mode 2 11: Mode 3
5	SM1_3	Multi-processor communication Enable bit In Mode 0, SM1_3 must be set as 0; meanwhile, the multi-processor communication function is disabled. In Mode 1, 2, and 3, if SM1_3 = 1, the multi-processor communication function is enabled.
4	REN_1	Serial Reception Enable bit. Cleared by software to disable reception. REN_1 = 1, reception starts REN_1 = 0, reception sopped
3	TB8_1	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
2	RB8_1	In Mode 0, this bit is invalid. In Mode 1, if SM1_3 = 0, this bit is Stop bit. In Mode 2 or 3, this bit is the 9th receive bit during data receiving.
1	TI_1	Transmit Interrupt Flag. When an interrupt is complete, this bit will not be resorted to “0”, and it must be cleared by software. In Mode 0, this bit is set by hardware at the end of the 8th bit time, and meantime it can commence a TI_1 interrupt.

Bit Number	Bit Mnemonic	Description
		In Mode 1, 2, or 3, this bit is set by hardware at the end of transmitting Stop bit, and meantime it can commence a TI_1 interrupt.
0	RI_1	Receive Interrupt Flag. When an interrupt is complete, this bit will not be resorted to "0", and it must be cleared by software. In Mode 0, this bit is set by hardware at the end of the 8th bit time, and meantime it can commence a RI_1 interrupt. In Mode 1, 2, or 3, this bit is set by hardware at the end of receiving Stop bit, and meantime it can commence a RI_1 interrupt.

The Serial Interface 1 can operate in four modes, as described below.

SM1_1	SM1_2	Mode	Function	Baud Rate
0	0	0	Shift Register	Fosc/12
0	1	1	8-bit UART	Software programmed
1	0	2	8-bit UART	Fosc/32 or Fosc/64
1	1	3	9-bit UART	Software programmed

***Fosc = MCU clock**

For more information about four modes of Serial Interface 1, refer to the "**Serial Interface 0**" content which is mentioned earlier.

Serial Baud rate of UART1:

SBRG1_EN (SBRG1H.7)	SMOD2 (PCON.6)	Baud Rate for UART1
0	0	$\frac{1}{32}\times\frac{f_{osc}}{12\times(65536-RCAP2)}$
0	1	$\frac{1}{16}\times\frac{f_{osc}}{12\times(65536-RCAP2)}$
1	X	$\frac{f_{osc}}{16*(BRG\_M[10:0]+\frac{BRG\_F[3:0]}{16})}$

If SBRG1_EN (SBRG1H.7) = 1

UART1 Baud rate = $\frac{f_{osc}}{16*(BRG1\_M[10:0]+\frac{BRG\_F[3:0]}{16})}$

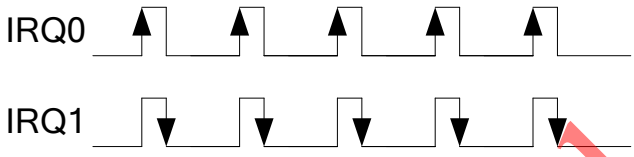
Baud rate supporting table:

	12 MHz				
Bits/sec	**Baud Rate Register**	**BRG_M**	**BRG_F**	**Actual**	**Error**
600	1250	1250	0	600	0.0%
1200	625	625	0	1200	0.0%
2400	312.5	312	8	2400	0.0%
4800	156.25	156	4	4800	0.0%
9600	78.125	78	2	9600	0.0%
14400	52.083	52	1	14405	0.04%
19200	39.0625	39	1	19200	0.0%
38400	19.531	19	8	38461	0.16%
57600	13	13	0	57692	0.16%
115200	6.5	6	8	115384	0.16%
230400	3.25	3	4	230769	0.16%

6.5 External Interrupt Request (IRQ)

- Supports 4 input Interrupts
- Supports single-side positive edge-triggered, negative edge-triggered, or positive edge and negative edge triggered simultaneously

Single side triggered:



Bidirectional triggered:

External Interrupt Request (IRQ) Control High Bytes Register EN_IRQ0 (XFR: 0x3A) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	W	W	W	W
Name	EVT_IRQ[3:0]				CLR_IRQ[3:0]			

Bit Number	Bit Mnemonic	Description
7-4	EVT_IRQ[3:0]	External Interrupt Request Status. Each bit is corresponded to the related IRQ status. 1: an interrupt trigger occurred in the corresponding pins. 0: an interrupt trigger not occurred in the corresponding pins.
3-0	CLR_IRQ[3:0]	External Interrupt Request Clear 1: writing one to the corresponding bits can clear the interrupt status 0: no action

External Interrupt Request (IRQ) Control Low Bytes Register EN_IRQ1 (XFR: 0x3B) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IRQ_CHG[3:0]				IRQ_EDGE[3:0]			

Bit Number	Bit Mnemonic	Description
7-4	IRQ_CHG[3:0]	External Interrupt Request Trigger setting 1: Bi-directional triggered 0: Single-side triggered (work together with IRQ_EDGE[3:0] to set positive or negative triggered)
3-0	IRQ_EDGE[3:0]	External Interrupt Request Trigger Edge setting 1: negative edge triggered 0: positive edge triggered

6.6 Pulse Width Modulation (PWM)

WT51F516 provides four 10-bit precise Pulse Width Modulation modules to generate periods and Duty cycles.

- Output Frequency is 1024 levels; Frequency range:

(a) If EN_PWM_IO[3:0] = 00, enable PWM output

(b) If PWM clock source = 1 MHz = 1 us

PWM period control value = 1 MHz / ((PWMCx +1)* 1024) = **1024us * (PWMCx+1)**

MAX period control value = 1024 us*1 = 1024 us = 0.975625 kHz

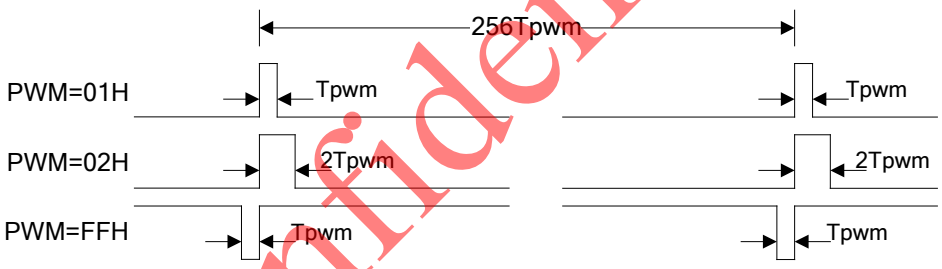
MIN period control value = 1024 us*128 = 13102 us = 7.629394531 Hz

PWM output clock (Min / Max)	12 MHz
PWM_BAS_CLK = 00 (12 MHz)	91.55 Hz / 11.72 kHz
PWM_BAS_CLK = 01 (6 MHz)	45.78 Hz / 5.86 kHz
PWM_BAS_CLK = 10 (3 MHz)	22.89 Hz / 2.93 kHz
PWM_BAS_CLK = 11 (1 MHz)	7.63 Hz / 0.98 kHz

- The resolutions of Duty and period and source clock are closely related to each other.

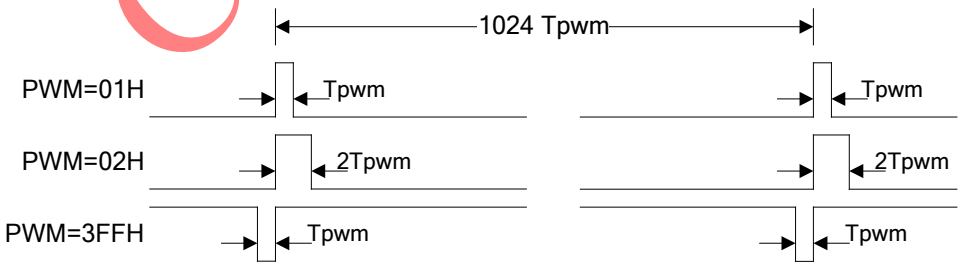
(a) Setting 8 bit PWM, PWM duty cycle formula. PWM duty cycle ranges from 0/256 to 255/256.

PWM output clock = PWM_BAS_CLK / ((PWM_CLKx +1)* 256)



(b) Setting 10 bit PWM, PWM duty cycle formula. PWM duty cycle ranges from 0/1024 to 1023/1024.

PWM output clock = PWM_BAS_CLK / ((PWM_CLKx +1)* 1024)



- For example, If source clock is IRC 12 MHz, Duty Resolution is 10 bit, then the periods range is limited within 11.7 kHz.
- Output type: push pull or open drain, can be configured by GPIOx_TYP[x]

PWM Control Register 0 PWM_CTL0 (XFR: 0x50) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM_EN[3:0]				PWM_BIT_SEL[3:0]			

Bit Number	Bit Mnemonic	Description
7-4	PWM_EN[3:0]	1: Enable PWM3 function 0: Disable PWM3 function
		1: Enable PWM2 function 0: Disable PWM2 function
		1: Enable PWM1 function 0: Disable PWM1 function
		1: Enable PWM0 function 0: Disable PWM0 function
3-0	PWM_BIT_SEL[3:0]	1: PWM3 = 8 bit 0: PWM3 = 10 bit
		1: PWM2 = 8 bit 0: PWM2 = 10 bit
		1: PWM1 = 8 bit 0: PWM1 = 10 bit
		1: PWM0 = 8 bit 0: PWM0 = 10 bit

PWM Control Register 1 PWM_CTL1 (XFR: 0x51) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved						PWM_BAS_CLK[1:0]	

Bit Number	Bit Mnemonic	Description
7-2	Reserved	-
1-0	PWM_BAS_CLK[1:0]	PWM Source clock selection 00: Source clock = RC 12 MHz 01: Source clock = RC 12 MHz /2 10: Source clock = RC 12 MHz /4 11: Source clock = RC 12 MHz /12

-: unimplemented.

PWM Clock Source Control Register 0 PWM_CLK0 (XFR: 0x52) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	PWM_CLK0[6:0]						

Bit Number	Bit Mnemonic	Description
7	Reserved	-
6-0	PWM0_CLK[6:0]	PWM_CLK0[6:0] sets the period control value of PWM0 PWM0 output clock = PWM_BAS_CLK/((PWM_CLKX + 1) * 256), clock source is selected by PWM_BAS_CLK[1:0].

-: unimplemented.

PWM Clock Source Control Register 1 PWM_CLK1 (XFR: 0x53) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	PWM_CLK1[6:0]						

Bit Number	Bit Mnemonic	Description
7	Reserved	-
6-0	PWM1_CLK[6:0]	PWM_CLK1[6:0] sets the period control value of PWM1 PWM1 output clock = PWM_BAS_CLK/((PWM_CLKX + 1) * 256), clock source is selected by PWM_BAS_CLK[1:0].

-: unimplemented.

PWM Clock Source Control Register 2 PWM_CLK2 (XFR: 0x54) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	-	PWM_CLK2[6:0]						

Bit Number	Bit Mnemonic	Description
7	Reserved	-
6-0	PWM2_CLK[6:0]	PWM_CLK2[6:0] sets the period control value of PWM2. PWM2 output clock = PWM_BAS_CLK/((PWM_CLKX + 1) * 256), clock source is selected by PWM_BAS_CLK[1:0].

-: unimplemented.

PWM Clock Source Control Register 3 PWM_CLK3 (XFR: 0x55) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	PWM_CLK3[6:0]						

Bit Number	Bit Mnemonic	Description
7	Reserved	-
6-0	PWM3_CLK[6:0]	PWM_CLK3[6:0] sets the period control value of PWM3 PWM3 output clock = PWM_BAS_CLK/((PWM_CLKX + 1) * 256), clock source is selected by PWM_BAS_CLK[1:0].

-: unimplemented.

PWM Duty Cycle Control Low Bytes Register0 PWM_DUTYL0 (XFR: 0x56) **Reset Value: 80h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM0_DUTY[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	PWM0_DUTY[7:0]	Sets the duty cycle output of PWM0 PWM0_DUTY[7:0] sets the duty cycle of PWM0, and is paired with PWM0_DUTY[9:8] to form a 10-bit of duty cycle control value.

PWM Duty Cycle High Bytes Register0 PWM_DUTYH0 (XFR: 0x57) Reset Value: 02h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved						PWM0_DUTY[9:8]	

Bit Number	Bit Mnemonic	Description
7-2	Reserved	-
1-0	PWM0_DUTY[9:8]	Sets the duty cycle output of PWM0 PWM0_DUTY[7:0] sets the duty cycle of PWM0, and is paired with PWM0_DUTY[7:0] to form a 10-bit of duty cycle control value.

-: unimplemented.

PWM Duty Cycle Control Low Bytes Register1 PWM_DUTYL1 (XFR: 0x58) Reset Value: 80h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM1_DUTY[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	PWM1_DUTY[7:0]	Sets the duty cycle output of PWM1 PWM1_DUTY[7:0] sets the duty cycle of PWM1, and is paired with PWM1_DUTY[9:8] to form a 10-bit of duty cycle control value.

PWM Duty Cycle Control High Bytes Register1 PWM_DUTYH1 (XFR: 0x59) Reset Value: 02h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved						PWM1_DUTY[9:8]	

Bit Number	Bit Mnemonic	Description
7-2	Reserved	-
1-0	PWM1_DUTY[9:8]	Sets the duty cycle output of PWM1 PWM1_DUTY[7:0] sets the duty cycle of PWM1, and is paired with PWM1_DUTY[15:8] to form a 10-bit of duty cycle control value.

-: unimplemented.

PWM Duty Cycle Control Low Bytes Register 2 PWM_DUTYL2 (XFR: 0x5A) Reset Value: 80h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM2_DUTY[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	PWM2_DUTY[7:0]	Sets the duty cycle output of PWM2 PWM2_DUTY[7:0] sets the duty cycle of PWM2, and is paired with PWM2_DUTY[9:8] to form a 10-bit of duty cycle control value.

PWM Duty Cycle Control High Bytes Register2 PWM_DUTYH2 (XFR: 0x5B) Reset Value: 02h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved						PWM2_DUTY[9:8]	

Bit Number	Bit Mnemonic	Description
7-2	Reserved	-
1-0	PWM2_DUTY[9:8]	Sets the duty cycle output of PWM2 PWM2_DUTY[7:0] sets the duty cycle of PWM2, and is paired with PWM2_DUTY[15:8] to form a 10-bit of duty cycle control value.

-: unimplemented.

PWM Duty Cycle Control Low Bytes Register3 PWM_DUTYL3 (XFR: 0x5C) Reset Value: 80h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM3_DUTY[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	PWM3_DUTY[7:0]	Sets the duty cycle output of PWM3 PWM3_DUTY[7:0] sets the duty cycle of PWM3, and is paired with PWM3_DUTY[9:8] to form a 10-bit of duty cycle control value.

PWM Duty Cycle Control High Bytes Register3 PWM_DUTYH3 (XFR: 0x5D) Reset Value: 02h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved						PWM3_DUTY[9:8]	

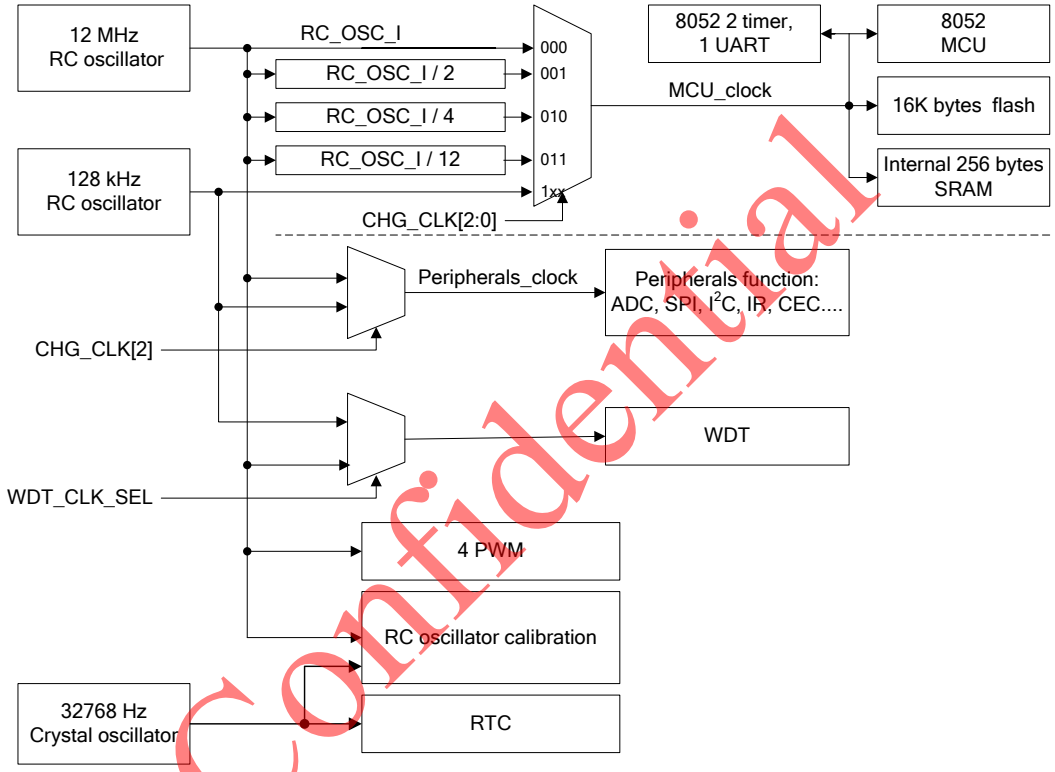
Bit Number	Bit Mnemonic	Description
7-2	Reserved	-
1-0	PWM3_DUTY[9:8]	Sets the duty cycle output of PWM3 PWM3_DUTY[7:0] sets the duty cycle of PWM3, and is paired with PWM3_DUTY[15:8] to form a 10-bit of duty cycle control value.

-: unimplemented.

6.7 Power Management

WT51F516 provides four operation modes, as listed below.

- Normal mode
- Idle mode: MCU_OFF
- Sleep mode: OSC_OFF
- Power-saving mode: PWR_SAVE



OFF mode

PWR_SAVE	OSC_OFF	MCU_OFF	RC12M_OSC_I	MCU_clock	Peripherals_ clock	Wake up wait MCU clock
0	0	0	ON	ON	ON	-
0	0	1	ON	OFF	OFF	4 clock
0	1	0	OFF	OFF	OFF	256 clock
1	0	0	OFF	OFF	OFF	ΔT+ 256 clock (*)

*** In Power-saving mode, it needs to wait for LDO 100ms and 256 RCOSC to return to the Normal mode after waking up.**

SYS System Control Register 0 SYS_CTL0 (XFR: 0x01) **Reset Value: 82H**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	-	R/W	R/W
Name	RST_NDF	OSC_OFF	OSC_OFF2	MCU_OFF	Reserved		OSC32K_EN	PWR_SAVE

Bit Number	Bit Mnemonic	Description
7	RST_NDF	1: Enable "NRST" Pin Digital Filter (default) 0: Disable "NRST" Pin Digital Filter
6	OSC_OFF	1: Power down mode, turn off RC clock source and system clock source (after waking up, MCU must wait for 256 RC OSC clock until it resume to work) 0: Normal mode
5	OSC_OFF2	1: Power down mode, turn off RC clock source and system clock source (after waking up, MCU must wait for 8 RC OSC clock until it resume to work) 0: Normal mode
4	MCU_OFF	1: MCU OFF mode, turn off system clock source, only turn on RC clock source (after waking up, MCU wait for 4RC OSC clock until it resume to work) 0: Normal mode
3-2	Reserved	-
1	OSC32K_EN	1: turn on external 32K oscillator, if no external 32K oscillator available in the system, this bit must be set as 0 0: turn off external 32K oscillator
0	PWR_SAVE	1: Power-saving mode 0: Normal mode

-: unimplemented.

SYS System Control Register 1 SYS_CTL1 (XFR: 0x02) **Reset Value: 20H**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	-	R/W	R/W	R/W
Name	Reserved	OSCOFF2_CLK_CTL	FLASH_POWER_CTL	CEC_IO_SEL	Reserved	CHG_CLK[2:0]		

Bit Number	Bit Mnemonic	Description
7	Reserved	-
6	OSCOFF2_CLK_CTL	1: wait for 32 RC OSC clock 0: wait for 8 RC OSC clock
5	FLASH_POWER_CTL	1: reduce flash power distribution time
4	CEC_IO_SEL	1: set CEC input pin being distributed to GPIOC5 0: set CEC input pin being distributed to GPIOA2
3	Reserved	-
2-0	CHG_CLK[2:0]	000: MCU clock = 12 MHz RC oscillator clock (default) 001: MCU clock = 12 MHz RC oscillator clock/2 010: MCU clock = 12 MHz RC oscillator clock/4 011: MCU clock = 12 MHz RC oscillator clock/12 1XX: MCU clock = 128 kHz RC oscillator clock

-: unimplemented.

SYS System Control Register 2 SYS_CTL2 (XFR: 0x03) **Reset Value: 00H**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	-	-	-	-	-	-
Name	DIS_GPC1_SMT	DIS_GPA7_SMT	Reserved					

Bit Number	Bit Mnemonic	Description
7	DIS_GPC1_SMT	GPIOC1 SMT input register control (for reducing power consumption) 1: Disable GPIOC1 SMT input 0: Enable GPIOC1 SMT input
6	DIS_GPA7_SMT	GPIOA7 SMT input register control (for reducing power consumption) 1: Disable GPIOA7 SMT input 0: Enable GPIOA7 SMT input
5-0	Reserved	-

-: unimplemented.

SYS System Control Register 3 SYS_CTL3 (XFR: 0x04) **Reset Value: 00H**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Flash_Protected				OSC12MRC_PD	OSC128KRC_PD	PD_BPLDO33	PD_LPLDO33

Bit Number	Bit Mnemonic	Description
7-4	FLASH_PRO	Write protection control bit FLASH_PRO[7:4] = 5: write allowed FLASH_PRO[7:4] = others: write not allowed
3	OSC12MRC_PD	1: Disable 12 MHz RC oscillator 0: Enable 12 MHz RC oscillator
2	OSC128KRC_PD	1: Disable 128 kHz RC oscillator 0: Enable 128 kHz RC oscillator
1	PD_BPLDO33	1: Turn off LDO33 (BIG LDO18) 0: Normal mode
0	PD_LPLDO33	1: Turn off LPLDO33 (Low power LDO33) 0: Normal mode

SYS System Control Register 4 SYS_CTL3 (XFR: 0x0F) **Reset Value: 20H**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PD_LVR	TEST[6:0]						

Bit Number	Bit Mnemonic	Description
7	PD_LVR	1: Disable LVR 0: Enable LVR
6-0	TEST[6:0]	Internal testing, must be set as 0x20h

SYS Wakeup Control Register 0 WAKEUP_EN0 (XFR: 0x20) **Reset Value: 00H**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	I2C_WAKE	WDT_WAKE	ACOMP_WAKE	RTC_500MS_WAKE	LVD_WAKE	Reserved		IR_WAKE

Bit Number	Bit Mnemonic	Description
7	I2C_WAKE	1: Enable I^2C Wakeup function 0: Disable I^2C Wakeup function
6	WDT_WAKE	1: Enable Watchdog Counter Wakeup function 0: Disable Watchdog Counter Wakeup function
5	ACOMP_WAKE	1: Enable Comparator Wakeup function 0: Disable Comparator Wakeup function
4	RTC_500MS_WAKE	1: Enable RTC 500ms Wakeup function 0: Disable RTC 500ms Wakeup function
3	LVD_WAKE	1: Enable Low Voltage Detection Wakeup function 0: Disable Low Voltage Detection Wakeup function
2-1	Reserved	-
0	IR_WAKE	1: Enable Infrared Receiver Wakeup function 0: Disable Infrared Receiver Wakeup function

-: unimplemented.

SYS Wakeup Control Register 1 WAKEUP_EN1 (XFR: 0x21) **Reset Value: 00H**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_WK[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOA_WK[7:0]	1: Enable GPIOA PORT pin Wakeup function 0: Disable GPIOA PORT pin Wakeup function

SYS Wakeup Control Register 2 WAKEUP_EN2 (XFR: 0x22) **Reset Value: 00H**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_WK[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOB_WK[7:0]	1: Enable GPIOB PORT pin Wakeup function 0: Disable GPIOB PORT pin Wakeup function

SYS Wakeup Control Register 3 WAKEUP_EN3 (XFR: 0x23) **Reset Value: 00H**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOC_WK[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOC_WK[7:0]	1: Enable GPIOC PORT pin Wakeup function 0: Disable GPIOC PORT pin Wakeup function

SYS Wakeup Trigger Register 0 WAKEUP_TOGGLE0 (XFR: 0x24) **Reset Value: 00H**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	-	-	R
Name	I2CPIN_TOG	WDT_EVT	ACOMP_TOG	RTC_500MS_TOG	LVD_EVT	Reserved		IR_TOG

Bit Number	Bit Mnemonic	Description
7	I2CPIN_TOG	1: I^2C Wakeup function Trigger Flag
6	WDT_EVT	1: Watchdog Counter Wakeup function Trigger Flag
5	ACOMP_TOG	1: Comparator Wakeup function Trigger Flag
4	RTC_500MS_TOG	1: RTC 500ms Wakeup function Trigger Flag
3	LVD_EVT	1: Low Voltage Detection Wakeup function Trigger Flag
2-1	Reserved	-
0	IR_TOG	1: Infrared Receiver Wakeup function Trigger Flag

-: unimplemented.

SYS Wakeup Trigger Register 1 WAKEUP_TOGGLE1 (XFR: 0x25) **Reset Value: 00H**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	GPIOA_TOG[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOA_TOG[7:0]	1: GPIOA PORT pin Wakeup function Trigger Flag

SYS Wakeup Trigger Register 2 WAKEUP_TOGGLE2 (XFR: 0x26) **Reset Value: 00H**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	GPIOB_TOG[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOB_TOG[7:0]	1: GPIOB PORT pin Wakeup function Trigger Flag

SYS Wakeup Trigger Register 3 WAKEUP_TOGGLE3 (XFR: 0x27) **Reset Value: 00H**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	GPIOC_TOG[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOC_TOG[7:0]	1: GPIOC PORT pin Wakeup function Trigger Flag

SYS Trigger Clear Control Register WAKEUP_CLR (XFR: 0x28) Reset Value: 00H

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	-	-	-	-	-	-	R
Name	CLR_IN_TOG	Reserved						IN_TOG

Bit Number	Bit Mnemonic	Description
7	CLR_IN_TOG	1: Clear all Trigger Flags
6-1	Reserved	-
0	IN_TOG	1: all Trigger Flags

-: unimplemented.

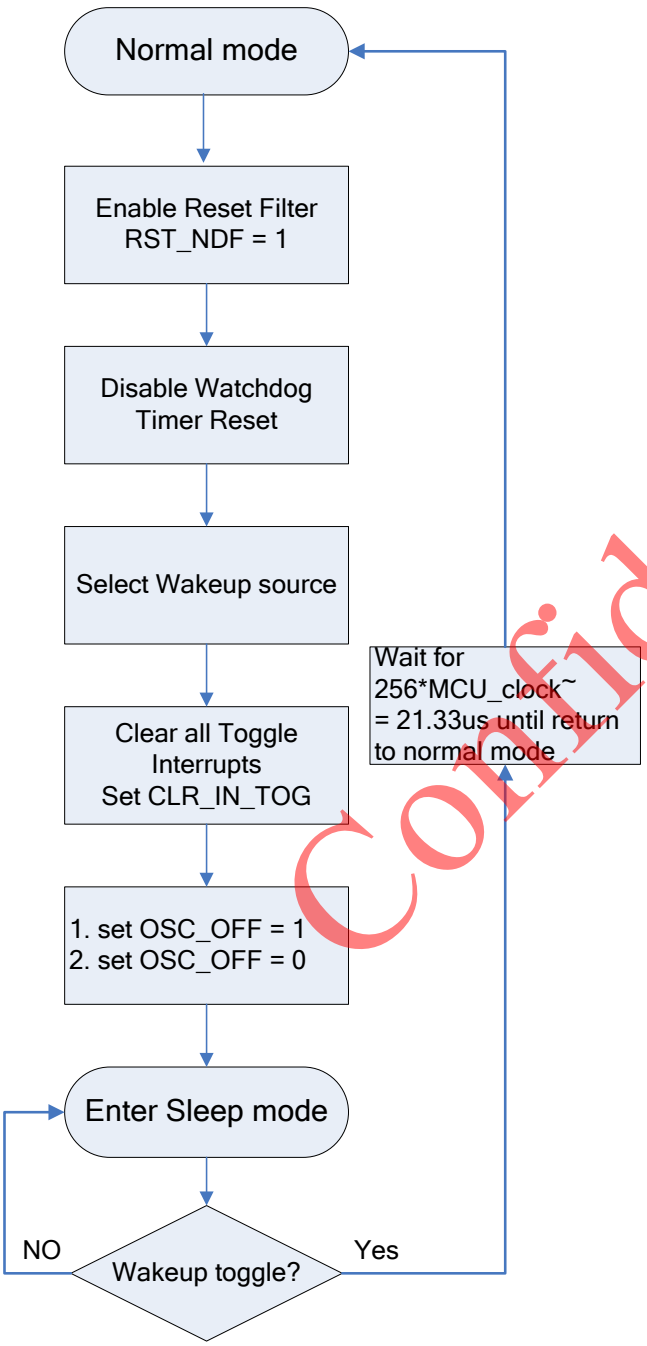
SYS Enhanced Timer/Counter Wakeup Control Register WAKEUP_ETM (XFR: 0x29) Reset Value: 00H

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	R/W	-	-	-	R
Name	Reserved			ETM_WAKE	Reserved			ETM_TOG

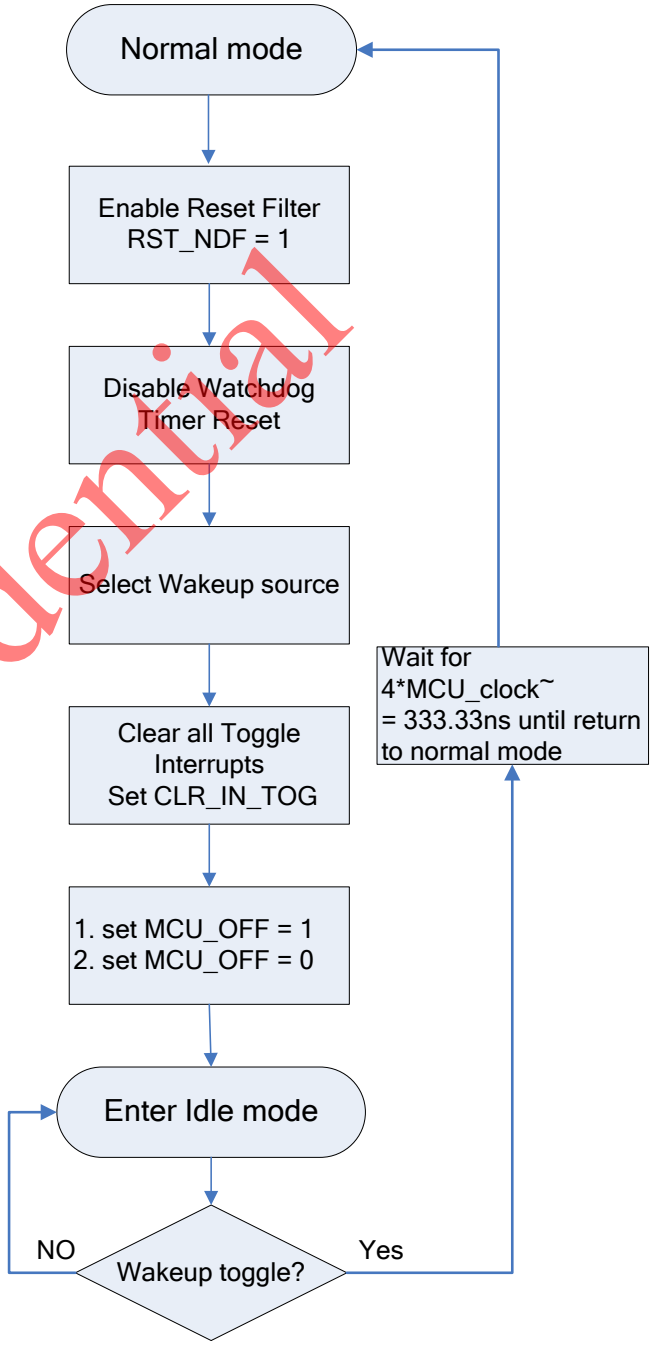
Bit Number	Bit Mnemonic	Description
7-5	Reserved	-
4	ETM_WAKE	1: Enable Enhanced Counter Wakeup function
3-1	Reserved	-
0	ETM_TOG	1: Enhanced Counter Trigger Flag

-: unimplemented.

WT51F516
Entering Sleep mode &
Wakeup procedures



WT51F516
Entering Idle mode &
Wakeup procedures



The setting of entering Sleep mode and Wakeup procedures:

(a) OSC_OFF wakeup sources include: I²C, WDT, ACOMP, RTC, LVD, GPIOA, GPIOB and GPIOC; Entering Sleep procedures:

(1) Set RST_NDFILT = 1
(2) Disable Watchdog Timer Reset
(3) Select Wakeup sources
(4) Set CLR_IN_TOG clear interrupt flag
(5) Set OSC_OFF =1, and then set OSC_OFF = 0
(6) Enter Sleep mode, wait for Wakeup Trigger
(7) As the signal is triggered, needs to wait for 256* MCU_clock until back to normal mode.

If XTAL clock is 12 MHz, MCU must wait for 21.33us

The setting of entering Idle mode and Wakeup procedures:

(b) MCU_OFF wakeup sources include: I²C, WDT, ACOMP, RTC, LVD, IR, GPIOA, GPIOB, GPIOC and Enhanced Timer; Entering Sleep procedures:

(1) Set RST_NDFILT = 1
(2) Disable Watchdog Timer Reset
(3) Select Wakeup sources
(4) Set CLR_IN_TOG
(5) Set MCU_OFF = 1, and then set MCU_OFF = 0
(6) Enter Sleep mode, wait for Wakeup Trigger
(7) As the signal is triggered, needs to wait for 4*MCU_clock until back to normal mode.

If XTAL clock is 12 MHz, MCU must wait for 333.33 ns

RTC_500MS_WAKE: Wakeup time selection requires setting register RTC_FS[2:0] (index BE-bit 2:0)
Any Sleep mode can be wakeup by RTC_500ms

RTC_FS[2:0]	Wake up time
000	No
001	2s
010	500ms
011	62.5ms
100	7.8125ms
101	0.9765625ms
110	488.28125us
111	15.2587890625us

6.8 12 MHz RC Oscillator Calibration

WT51F516 has a built-in 12 MHz RC oscillator to reduce the cost of external crystal oscillator. For more precise system clock, it is a better choice to use 32.768 kHz (crystal oscillator) to calibrate internal RC 12 MHz oscillator. (Calibration can reach ±1% at -40℃ ~ +85℃)

Internal Oscillator Counter Data High Bytes Register RC_CAL [9:2] (XFR: 0x2A) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	RC_CAL [9:2]							

Bit Number	Bit Mnemonic	Description
7-0	RC_CAL[9:2]	The counting value RC_CAL [9:2] of internal 12 MHz RC oscillator, is paired with RC_CAL [1:0] to form a 10-bit counting value

Internal Oscillator Counter Data Low Bytes Register RC_CAL [1:0] (XFR: 0x2B) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R	R
Name	Reserved						RC_CAL [1:0]	

Bit Number	Bit Mnemonic	Description
7-2	Reserved	-
1-0	RC_CAL [1:0]	The counting value RC_CAL [1:0] of internal 12 MHz RC oscillator, is paired with RC_CAL [9:2] to form a 10-bit counting value

-: unimplemented.

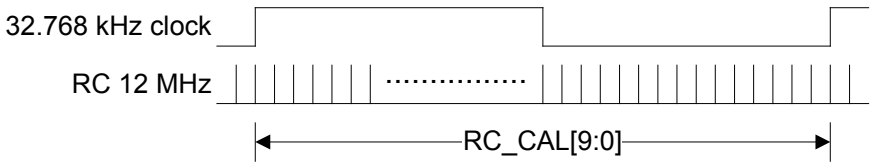
Internal Oscillator Calibration Control Register RC_IADJ (XFR: 0x2C) **Reset Value: 40h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	RC_IADJ_C[2:0]			RC_IADJ_F[3:0]			

Bit Number	Bit Mnemonic	Description
7	Reserved	-
6-4	RC_IADJ_C[2:0]	Each level 8% coarse adjustment of the Internal RC oscillator frequency (default value ''100h'), 8 levels in total.
3-0	RC_IADJ_F[3:0]	Each level 0.5% fine adjustment of the internal RC oscillator frequency (default value '0000h'), 15 levels in total.

-: unimplemented.

Note: Internal Oscillator Adjustment Register RC_IADJ_C[2:0] & RC_IADJ_F[3:0] is allowed to adjust the control circuit of IRC 12 MHz directly.



Calibration Theory:

When the external 32.768 kHz oscillator is used, it is available to count in the fixed width of precise 32.768 kHz by internal RC 12 MHz. Then with the counting value we got, we can make compensation by controlling the Internal Oscillator Adjust Registers RC_IADJ_C[2:0] & RC_IADJ_F[3:0], reaching ±1%.

The range of coarse adjustment and fine adjustment:

Coarse adjustment: the actual internal RC frequency ± (internal RC frequency * 0.08); RC_IADJ_C[2:0] ranges from 000h ~ 111h, and the middle value is 100h.

Fine adjustment: the actual internal RC frequency ± (internal RC frequency * 0.005); RC_IADJ_F[3:0] ranges from 0000h ~ 1111h, and the middle value is 1000h.

RC_CAL[9:0]	External 32.768 kHz Sampled (Hz)	Target Value (Hz)	Tolerance %
360	11796480	12000000	+1.70
361	11829248	12000000	+1.42
362	11862016	12000000	+1.15
363	11894784	12000000	+0.88
364	11927552	12000000	+0.60
365	11960320	12000000	+0.33
366	11993088	12000000	+0.06
367	12025856	12000000	-0.22
368	12058624	12000000	-0.49
369	12091392	12000000	-0.76
370	12124160	12000000	-1.03

Note:

1. **When WT51F516 is waken up from sleep mode (RC bias is turned on), RC oscillator calibration function needs to wait for at least 83.3ns (at 12 MHz) to return to normal mode.**
2. **As soon as the RC oscillator calibration function is enabled, read RC_CAL [9:2] & RC_CAL [1:0] registers twice, then confirm the data is the same to proceed with the calibration process.**
3. **If RC_CAL [9:0] Internal Oscillator Counter Data Register is 511(0x1FF), indicating that no external oscillator or without enabling external oscillator.**
4. **When reset, WT51F516 will auto-reload the calibration value of RC 12 MHz into internal oscillator adjustment register.**

6.9 Watchdog Timer (WDT)

Watchdog Timer can be used to detect CPU failures, such as the software deadlock circles caused by noises, voltage disturbance, or power off etc. When an internal counter of the Watchdog Timer overflows, a reset signal will be generated then reset the CPU.

Watchdog Timer is not similar to the general-purpose 8052 Timer 0/1/2. To prevent a reset occurred on Watchdog Timer, which can be cleared by software before important path of program. When unpredictable reset occurred, user should check the WDT_RST_EVT bit in Reset Flag Register to judge if the previous reset is occurred by Watchdog Timer.

- Clock sources of Watchdog Timer: Internal RC 12 MHz or Internal RC 128 kHz
- Reset Time: 32.77ms, 65.54ms, 1.05S, 2.10S, 8.23S

Watchdog Timer Control Register 0 WDT_CTL0 (XFR: 0x08) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	-	-	-	-	-	R
Name	DIS_WDT	WDT_CLK_SEL	Reserved					WDT_RST_EVT

Bit Number	Bit Mnemonic	Description
7	DIS_WDT	Watchdog Timer switch 1: Disable Watchdog Timer at the same time clear counts 0: Enable Watchdog Timer
6	WDT_CLK_SEL	Watchdog Timer Clock source selection 1: Watchdog Timer uses internal 12 MHz RC oscillator 0: Watchdog Timer uses internal 128 kHz RC oscillator
5-1	Reserved	-
0	WDT_RST_EVT	1: Reset sources is Watchdog If reset, this bit is set as 1 by hardware; and set as DIS_WDT as 1 by firmware and cleared as 0.

-: unimplemented.

Note:

1. Regarding the Internal 12 MHz/32K RC oscillator frequency tolerance, please refer to Electrical Characteristics sections.

2. Set DIS_WDT bit will clear WDT_DET_EVT bit, and WDT will reset time.

Watchdog Timer Control Register 1 WDT_CTL1 (XFR: 0x09) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	R/W	R/W	R/W
Name	Reserved					WDT_RST[2:0]		

Bit Number	Bit Mnemonic	Description
7-3	Reserved	-
2-0	WDT_RST[2:0]	Watchdog Reset Time setting When the Watchdog uses internal RC 12 MHz oscillator: 000: 1.05s 001: 2.10s 010: 32.77ms 100: 65.54ms 1XX: 8.23s When the Watchdog uses internal RC 128 kHz oscillator: 000: 1.02s 001: 2.05s 010: 32.0ms 100: 64.0ms 1XX: 8.13s

-: unimplemented.

Watchdog Timer Control Register 2 WDT_CTL2 (XFR: 0x0A) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	R/W	R/W	R/W
Name	Reserved					WDT_DET[2:0]		

Bit Number	Bit Mnemonic	Description
7-3	Reserved	-
2-0	WDT_DET[2:0]	Watchdog Wakeup Time setting When the Watchdog uses internal RC 12 MHz oscillator: 000: 1.05s 001: 2.10s 010: 32.77ms 100: 65.54ms 1XX: 5.24s When the Watchdog uses internal RC 128 kHz oscillator: 000: 1.02s 001: 2.05s 010: 32.0ms 100: 64.0ms 1XX: 5.12s

-: unimplemented.

6.10 Consumer Electronics Control (HDMI CEC)

Consumer Electronics Control (CEC) is an optional feature within the HDMI specification. It can simplify the operation of the Digital Home, such as using the remote control to control the digital products which support HDMI-CEC. CEC is now supported by most of the manufacturers under their own proprietary names, such as Samsung's Anynet+, LG's SIMPLINK, Panasonic's VIERA Link, Sony's BRAVIA SYNC, Sharp's Fami Link, and etc. The CEC signal allows consumers to control the digital products which is connected with HDMI.

MCU hardware will store CEC data in the buffer register (1 byte) and then access the data by software, which implements CEC package receive/transmit and debugging, enabling customers to easily design CEC into their end equipment.

CEC Control Register (XFR: 0x70) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	-	-	R	W	W	-	-
Name	EN_CEC	Reserved		CEC_BUSY	CEC_L_4800US	CEC_L_3600US	Reserved	

Bit Number	Bit Mnemonic	Description
7	EN_CEC	CEC switch 1: Enable HDMI-CEC 0: Disable HDMI-CEC
6-5	Reserved	-
4	CEC_BUSY	If CEC is in busy status 1: CEC is busy, indicating signals are transmitting 0: CEC is not busy, indicating no signals are transmitting
3	CEC_L_4800US	1: Force CEC line = "L" 4.8ms, and be cleared automatically 0: Disable forcing CEC line = "L" 4.8ms
2	CEC_L_3600US	1: Force CEC line = "L" 3.6ms, and be cleared automatically 0: Disable forcing CEC line ="L" 3.6ms
1-0	Reserved	-

-: unimplemented.

CEC Initiator Register (XFR: 0x71) **Reset Value: 10h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R	-	-	-	-	-
Name	CEC_TR	CEC_O_EOM	CEC_RXACK	Reserved				

Bit Number	Bit Mnemonic	Description
7	CEC_TR	1: Enable Initiator state and transmit CEC data 0: Enable Follower state and receive CEC data
6	CEC_O_EOM	1: Transmit EOM bit = 1 indicating transmission is finished 0: Transmit EOM bit = 0 indicating transmission is still proceeding
5	CEC_RXACK	Receive ACK bit status 1: Receive NACK 0: Receive ACK
4-0	Reserved	-

-: unimplemented.

CEC Follower Register (XFR: 0x72) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R/W	R/W	-	-	-	-
Name	CEC_I_STR	CEC_I_EOM	CEC_TXACK	CEC_NACK_INT	Reserved			

Bit Number	Bit Mnemonic	Description
7	CEC_I_STR	1: Receive CEC Start bit 0: Did not receive CEC Start bit
6	CEC_I_EOM	1: Receive EOM bit = 1 0: Receive EOM bit = 0
5	CEC_TXACK	1: When NACK, transmit ACK bit = 1 0: When ACK, transmit ACK bit = 0
4	CEC_NACK_INT	1: Enable the interrupt of CEC_RX_INT which occurred even the next CEC signal appeared during transmitting NACK 0: Disable the interrupt of CEC_RX_INT which occurred even the next CEC signal appeared during transmitting NACK
3-0	Reserved	-

-: unimplemented.

CEC Interrupt Control Register (XFR: 0x73) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	-	-
Name	CEC_INT	CEC_TX_INT	CEC_RX_INT	CEC_DLOSS	CEC_TM_OUT	CEC_LINE_ERROR	Reserved	

Bit Number	Bit Mnemonic	Description
7	CEC_INT	1: CEC interrupt occurred. 0: no CEC interrupt occurred.
6	CEC_TX_INT	1: interrupt occurred after data transmitting finished (after transmitting one CEC byte) 0: no event transmit interrupt
5	CEC_RX_INT	1: interrupt occurred after data receiving finished (after receiving one CEC byte) 0: No event receive interrupt
4	CEC_DLOSS	1: In transmitting, the Interrupt event caused by data loss which resulted from being sent with other CEC signals simultaneously 0: No event data loss interrupt
3	CEC_TM_OUT	1: In receiving, the interrupt event resulted from only receiving some bit instead of receiving the whole byte (one bit time is over 6.144ms) 0: No time out interrupt occurred.
2	CEC_LINE_ERROR	1: In receiving, the interrupt event resulting from receiving error bits (bit width < 1.9ms) 0: No event line error interrupt
1-0	Reserved	-

-: unimplemented.

CEC Clear Interrupt Register (XFR: 0x74) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	W	W	W	W	W	-	-
Name	Reserved	CLR_TX_INT	CLR_RX_INT	CLR_DLOSS	CLR_TM_OUT	CLR_LINE_ERROR	Reserved	

Bit Number	Bit Mnemonic	Description
7	Reserved	-
6	CLR_TX_INT	1: Clear transmit interrupt 0: no action
5	CLR_RX_INT	1: Clear receive interrupt 0: no action
4	CLR_DLOSS	1: Clear the Interrupt event caused by data loss which resulted from being sent with other CEC signals simultaneously during transmitting 0: no action
3	CLR_TM_OUT	1: Clear the interrupt event resulted from only receiving some bit instead of receiving the whole byte during receiving 0: no action
2	CLR_LINE_ERROR	1: Clear the interrupt event resulting from receiving error bits during receiving 0: no action
1-0	Reserved	-

-: unimplemented.

1. Clearing interrupt needs to write 1.

2. If CEC_DLOSS == 1, then

(a) Initiator state will go to IDLE, and CEC_TR = 0.

(b) If Initiator wants to send next data package, it needs to wait "signal free time" (refer to HDMI specification) and re-set CEC_TR.

3. If CEC_LINE_ERROR == 1 or CEC_TM_OUT == 1, it needs to set CEC_L4800US = 1.

CEC Transmit Buffer Register (XFR: 0x75) **Reset Value: FFh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	CEC_DTX[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	CEC_DTX[7:0]	CEC transmit buffer register

CEC Receive Buffer Register (XFR: 0x76) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CEC_DRX[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	CEC_DRX[7:0]	CEC receive buffer register

6.11 Real Time Clock

RTC can work by backup battery or super-cap when the system power is off, and transmit 8-bit BCD code data to MCU. It provides 7 kinds of time value including Years, Months, Weeks, Days, Hours, Minutes, and Seconds, and enabling users to set Timer Switch device by this calendar.

The user is allowed to fill in the setting time into the corresponding register. Automatic timing starts upon turning on the RTC function. It is easy to get the current time by reading out the data stored in the corresponding register.

1. If VDD_RTC is connected with super-cap, the MCU must wait for VDD_RTC power being stable, then the MCU can read/write RTC registers. MCU must wait to check whether the written data and the read data are equal. If the data is equal, MCU starts to read/write all RTC registers.
2. Before using the RTC function, MCU needs to reset RTC module by setting RTC_RESET register, with procedures as below:
   1. Set RTC_RESET = 1 → 2. Set RTC_RESET = 0 → 3. Set RTC_EN = 1, enable RTC and work starts

RTC Control Register 0 RTC_CTRL0 (XFR: 0x38) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R/W	R/W	R/W	-	-	-	W
Name	RTC_1S	RTC_CS	RTC_EN	RTC_RESET	Reserved			CLR_RTC_1S

Bit Number	Bit Mnemonic	Description
7	RTC_1S	1: RTC 1s interrupt flag
6	RTC_CS	1: Enable RTC and R/W is allowed 0: Disable RTC and R/W is allowed
5	RTC_EN	1: Enable RTC and read is allowed 0: Disable RTC and read is allowed
4	RTC_RESET	1: RTC reset
3-1	Reserved	-
0	CLR_RTC_1S	1: RTC 1s interrupt flag

-: unimplemented.

RTC Second Control Register RTC_SEC (XFR: 0xB0) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	RTC_SEC[6:0]						

Bit Number	Bit Mnemonic	Description
7	Reserved	-
6-0	RTC_SEC[6:0]	Seconds coded in BCD ranging from 0 ~ 59

-: unimplemented.

RTC Minute Control Register RTC_MIN (XFR: 0xB1) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	RTC_MIN[6:0]						

Bit Number	Bit Mnemonic	Description
7	Reserved	-
6-0	RTC_MIN[6:0]	Minutes coded in BCD ranging from 0 ~ 59

-: unimplemented.

RTC Hour Control Register RTC_HOUR (XFR: 0xB2) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved		RTC_HOUR[5:0]					

Bit Number	Bit Mnemonic	Description
7-6	Reserved	-
5-0	RTC_HOUR[5:0]	Hours coded in BCD ranging from 0 ~ 23

-: unimplemented.

RTC Day Control Register RTC_DAY (XFR: 0xB3) **Reset Value: 01h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved		RTC_DAY[5:0]					

Bit Number	Bit Mnemonic	Description
7-6	Reserved	-
5-0	RTC_DAY[5:0]	Days coded in BCD ranging from 1 ~ 31

-: unimplemented.

RTC Week Control Register RTC_WEEK (XFR: 0xB4) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	R/W	R/W	R/W
Name	Reserved					RTC_WEEK[2:0]		

Bit Number	Bit Mnemonic	Description
7-3	Reserved	-
2-0	RTC_WEEK[2:0]	000: Sunday 001: Monday 010: Tuesday 011: Wednesday 100: Thursday

Bit Number	Bit Mnemonic	Description
		101: Friday 110: Saturday

-: unimplemented.

RTC Month Control Register RTC_MONTH (XFR: 0xB5) **Reset Value: 01h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				RTC_MONTH[3:0]			

Bit Number	Bit Mnemonic	Description
7-4	Reserved	-
3-0	RTC_MONTH[3:0]	0000: January 0001: February 0010: March 0011: April 0100: May 0101: June 0110: July 0111: August 1000: September 1001: October 1011: November 1100: December

-: unimplemented.

RTC Year Control Register RTC_YEAR (XFR: 0xB6) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	RTC_YEAR[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	RTC_YEAR[7:0]	Years coded in BCD ranging from 0 ~ 99

RTC Backup Control Register 1 RTC_BAKUP1 (XFR: 0xB8) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	RTC_BAKUP1							

Bit Number	Bit Mnemonic	Description
7-0	RTC_BAKUP1	Backup data register 1

RTC Backup Control Register 2 RTC_BAKUP2 (XFR: 0xB9) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	RTC_BAKUP2							

Bit Number	Bit Mnemonic	Description
7-0	RTC_BAKUP2	Backup data register 2

RTC Backup Control Register 3 RTC_BAKUP3 (XFR: 0xBA) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	RTC_BAKUP3							

Bit Number	Bit Mnemonic	Description
7-0	RTC_BAKUP3	Backup data register 3

RTC Backup Control Register 4 RTC_BAKUP4 (XFR: 0xBB) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	RTC_BAKUP4							

Bit Number	Bit Mnemonic	Description
7-0	RTC_BAKUP4	Backup data register 4

RTC Control Register 1 RTC_CTRL1 (XFR: 0xBC) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				AMP[3:0]			

Bit Number	Bit Mnemonic	Description
7-4	Reserved	-
3-0	AMP[3:0]	Select adjusting the amplified current of 32.768 kHz

-: unimplemented.

RTC Control Register 2 RTC_CTRL2 (XFR: 0xBD) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	RTC_CA[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	RTC_CA[7:0]	Calibration bit

RTC Control Register 3 RTC_CTRL3 (XFR: 0xBE) **Reset Value: 81h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	-	-	R/W	R/W	R/W	R/W
Name	RTC_PDOSC	RTC_STOP	Reserved		RTC_PDOSCSU	RTC_FS[2:0]		

Bit Number	Bit Mnemonic	Description
7	RTC_PDOSC	1: Disable 32.768 kHz oscillator 0: Enable 32.768 kHz oscillator
6	RTC_STOP	1: Disable RTC 0: Enable RTC
5-4	Reserved	-
3	RTC_PDOSCSU	1: turn off 32.768 kHz start oscillator circuit
2-0	RTC_FS[2:0]	Output frequency 000: no output 001: 0.25 Hz 010: 1 Hz 011: 8 Hz 100: 64 Hz 101: 512 Hz 110: 1024 Hz 111: 32768 Hz

-: unimplemented.

RTC Control Register 4 RTC_CTRL4 (XFR: 0xBF) **Reset Value: 62h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	-	R/W	R/W
Name	RX[3:0]				Reserved		DRV2(*2)	DRV1

Bit Number	Bit Mnemonic	Description
7-4	RX[3:0]	Bias resistor setting 0000: Don't use 0001: 300k 0010: 350K 0011: 400K 0100: 450K 0101: 500K 0110: 550K 0111: 600K 1000: 650K 1001: 700K 11XX: 750K
3-2	Reserved	-
1	DRV2	Oscillator current control 1: amplifier current
0	DRV1	Oscillator driving amplified control 1: amplified driving ability

-: unimplemented.

(1) If oscillator is stable, MCU can set RTC_PDOSCSU = 1 to reduce power consumption
(2) Set DRV2 = 1 to speed up oscillator, when oscillator is stable, MCU can set DRV2 = 0 to reduce power consumption.

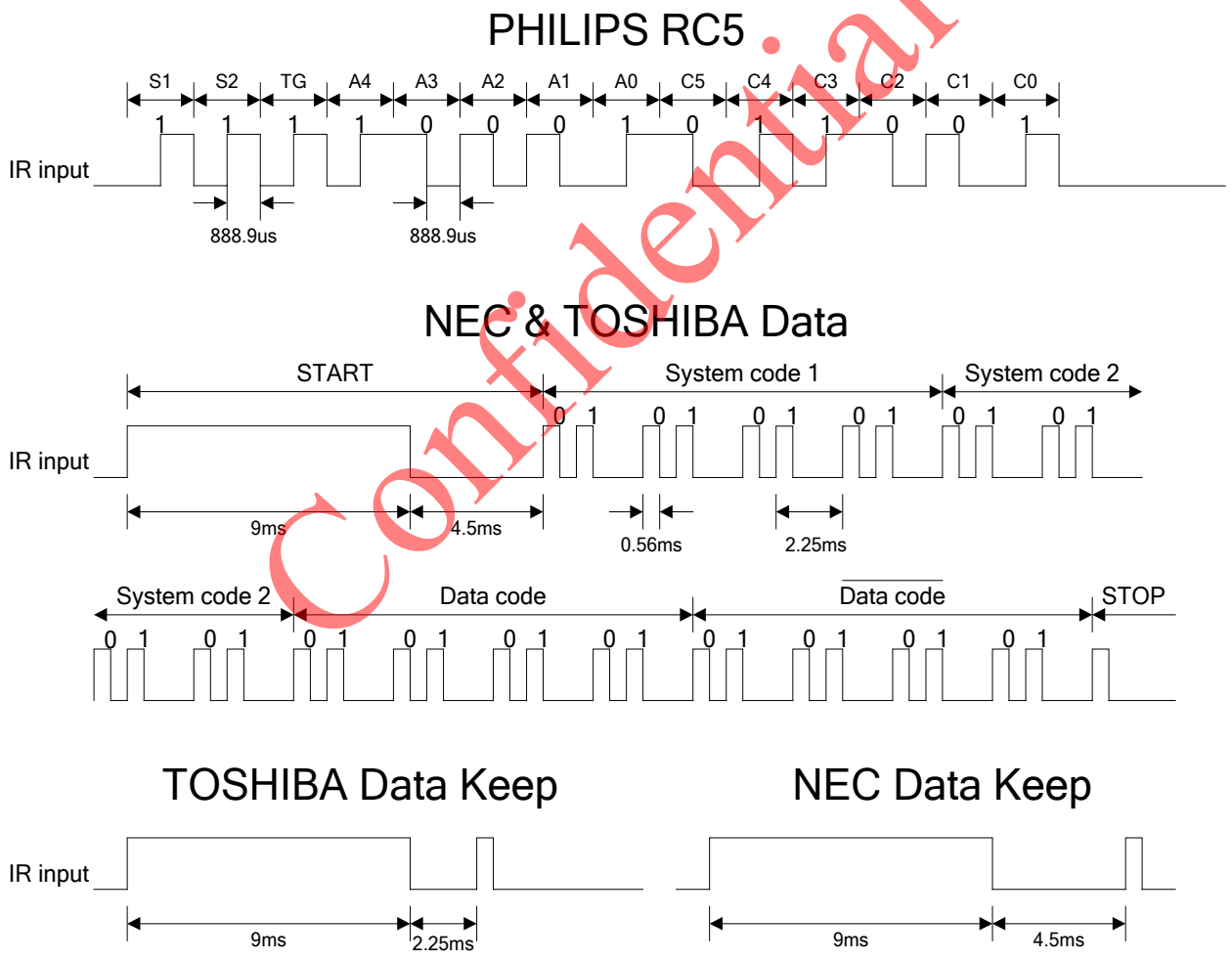
6.12 Infrared Receiver

The infrared is one kind of wireless communications that has been developed and utilized widely in home appliances, such as televisions, stereos, VCRs, air conditioners, DVDs, and etc.

In serial communication we usually speak of “marks” and “spaces”. The “space” is the default signal, which is the off state in the transmitter case. No IR LED is emitted during the “space” state. During the “mark” state, the IR LED is pulsed on and off at a particular frequency. Frequencies between 30 kHz and 60 kHz are commonly used in consumer electronics.

After the IR signal received by IR receiver been demodulated, MCU is allowed to set internal timing and to calculate the interval time of each rising and falling edge by firmware. Thus, figure out the IR format meets each manufacturer’s standard.

There are several IR Protocols on the market, such as NEC, RC5, RC6, Toshiba, Sharp, and etc. with the output waveforms illustrated as below.



IR Timing Table

		STARTH	STARTL	pulse	H period	L period
TC9290	data	9	4.5	0.56	2.25	1.125
(TC9243)	keep	9	4.5	0.56	2.25	
NEC uPD6P5	data	9	4.5	0.56	2.25	1.125
	keep	9	2.25	0.56		
Philips RC5	data	0.889	0.889	0.889	0.889	0.889

Infrared Control Register IR_EN0 (XFR: 0x60) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	EN_IR	IR_SEDG	IR_RF	EN_OV_INT	PRE_SCAL[2:0]			CLR_IR_INT

Bit Number	Bit Mnemonic	Description
7	EN_IR	1: Enable infrared control 0: Disable infrared control
6	IR_SEDG	External Interrupt Request Trigger setting 1: both sides triggered 0: single side triggered (based on IRQ_EDGE[3:0] setting positive-edge or negative-edge triggered)
5	IR_RF	External Interrupt Request trigger edge setting 1: negative-edge triggered 0: positive-edge triggered
4	EN_OV_INT	1: Enable overflow interrupt 0: Disable overflow interrupt
3-1	PRE_SCAL[2:0]	Infrared remote control sampling time setting 000: 1us 001: 8us 010: 32us 011: 64us 100: 128us 101: 256us 110: 512us 111: 1024us
0	CLR_IR_INT	Infrared remote control interrupt clear 1: the interrupt status can be cleared by setting the corresponding bit “1” 0: no action

Infrared Interrupt Register IR_EN1 (XFR: 0x61) **Reset Value: 04h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	R	R	R
Name	Reserved					IR_HL	IR_OVFLW	IR_INT

Bit Number	Bit Mnemonic	Description
7-3	Reserved	-

Bit Number	Bit Mnemonic	Description
2	IR_HL	IR pin input status 1: high level 0: low level
1	IR_OVFLW	1: IR overflow interrupt flag
0	IR_INT	1: IR interrupt = edge trigger + over low 0: no interrupt occurred

-: unimplemented.

Infrared Counter Register IR_CNT2 (XFR: 0x62) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	IR_CNT[7:0]							

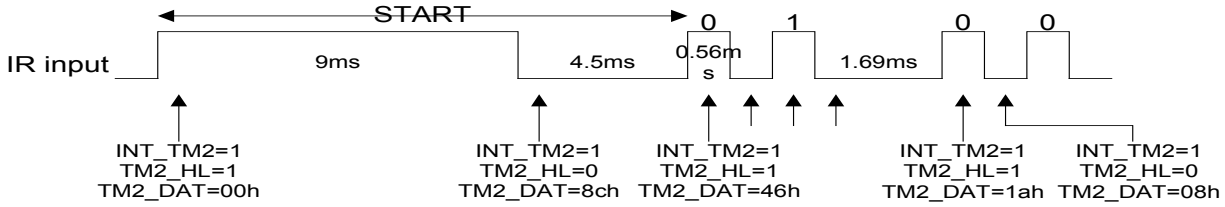
Bit Number	Bit Mnemonic	Description
7-0	IR_CNT[7:0]	IR counting value

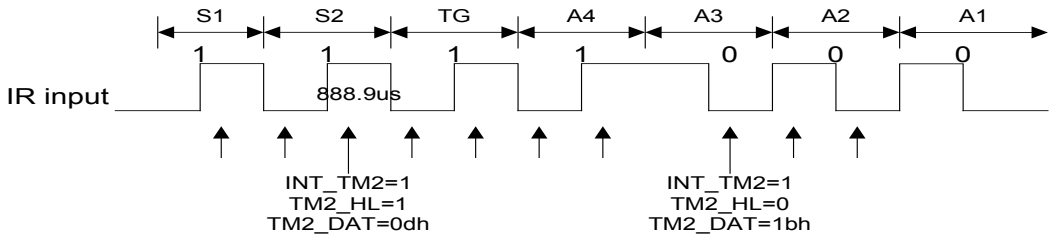
Infrared Digital Filter Register IR_FILTER[3:0] (XFR: 0x63) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				IR_FILTER[3:0]			

Bit Number	Bit Mnemonic	Description
7-4	Reserved	-
3-0	IR_FILTER[3:0]	IR digital filter = 0h: 2 X 84 ns = 168 ns digital filter = 1h: 1 X 32 us = 32 us digital filter = Fh: 15 X 32 us = 480 us digital filter

-: unimplemented.





6.13 I²C Serial Interface

I²C module uses SCL (clock) and SDA (data) wires to connect with other I²C interfaces, the transmission is determined by the software programmed I²C_CLK[1:0] in XFR, and is able to reach 400 KBpS (maximum).

I²C module also provides Slave mode.

Slave I²C Control Register I²C_CTL (XFR: 0xA0) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	-	-	R/W
Name	SIIC_EN	EN_INT_RT	EN_INT_STOP	EN_INT_RSTR	SIIC_WAIT	Reserved		SIIC_TXNAK

Bit Number	Bit Mnemonic	Description
7	SIIC_EN	1: Enable I²C function 0: Disable I²C function
6	EN_INT_RT	1: Enable I²C R/W bit 0: Disable I²C R/W bit
5	EN_INT_STOP	1: Enable I²C Transmit Stop bit 0: Disable I²C Transmit Stop bit
4	EN_INT_RSTR	1: Enable I²C Transmit Start bit 0: Disable I²C Transmit Start bit
3	SIIC_WAIT	1: Enable Slave I²C pull SCL low after the 9th bit 0: Disable Slave I²C pull SCL low after the 9th bit
2-1	Reserved	-
0	SIIC_TXNAK	In Slave mode, the corresponding bit before receiving next data 1: return NACK 0: return ACK

-: unimplemented.

Slave I²C Interrupt Register I²C_INT (XFR: 0xA1) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				TX_INT_NUM[1:0]		RX_INT_NUM[1:0]	

Bit Number	Bit Mnemonic	Description
7-4	Reserved	-
3-2	TX_INT_NUM[1:0]	Set the quantity of data transmitting bytes at each interrupt 00: 1-byte interrupt 01: 2-byte interrupt 10: 4-byte interrupt 11: 8-byte interrupt
1-0	RX_INT_NUM[1:0]	Set the quantity of data receiving bytes at each interrupt 00: 1-byte interrupt 01: 2-byte interrupt 10: 4-byte interrupt 11: 8-byte interrupt

-: unimplemented.

Slave I²C Flag Clear Register I²C_FLG_CLR[7:0] (XFR: 0xA2) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	-	-	-	-	-
Name	SIIC_CLR_RT	SIIC_CLR_STOP	SIIC_CLR_RSTR	Reserved				

Bit Number	Bit Mnemonic	Description
7	SIIC_CLR_RT	1: Clear transmit/receive interrupt
6	SIIC_CLR_STOP	1: Clear Stop phase interrupt in Slave mode
5	SIIC_CLR_RSTR	1: Clear Start phase interrupt in Slave mode
4-0	Reserved	-

-: unimplemented.

Slave I²C Flag Register I²C_FLG[7:0] (XFR: 0xA3) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	-	R	R	R
Name	SIIC_AL_RDY	SIIC_INT_RT	SIIC_INT_STOP	SIIC_INT_RSTR	Reserved	SIIC_FIRST	SII_ALRW	SII_RXNAK

Bit Number	Bit Mnemonic	Description
7	SIIC_AL_RDY	1: interrupt status when I^2C Receive/Transmit interrupt the 9th bit or Slave Stop phase
6	SIIC_INT_RT	1: interrupt status when I^2C Receive/Transmit interrupt the 9th bit
5	SIIC_INT_STOP	1: interrupt status when I^2C Slave mode Stop phase
4	SIIC_INT_RSTR	1: interrupt status when I^2C Slave mode Restart phase
3	Reserved	-
2	SIIC_FIRST	Slave mode First phase. This is the first byte from Master I^2C with specific Slave Address.
1	SII_ALRW	R/W mode phase in Slave mode（(the 8th bit of the first byte） 1: Slave I²C is in Transmit mode 0: Slave I²C is in Receive mode
0	SII_RXNAK	The acknowledge phase bit in Slave transmit mode 1: Master returns NACK 0: Master returns ACK

Slave I²C Address Register I²C_SADR (XFR: 0xA4) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
Name	SIIC_SADR[6:0]							Reserved

Bit Number	Bit Mnemonic	Description
7-1	SIIC_SADR[6:0]	Slave address
0	Reserved	-

-: unimplemented.

Slave I²C Index Clear Control Register I²C_INDEX_CLR (XFR: 0xA8) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	-	-	-	-	-	-
Name	CLR_IIC_TX_FIFO_INDEX	CLR_IIC_RX_FIFO_INDEX	Reserved					

Bit Number	Bit Mnemonic	Description
7	CLR_IIC_TX_FIFO_INDEX	Clear I²C Transmit index
6	CLR_IIC_RX_FIFO_INDEX	Clear I²C Receive index
5-0	Reserved	-

-: unimplemented.

Slave I²C TX FIFO Control Register I²C_TXFIFO_INDEX (XFR: 0xA9) **Reset Value: 80h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	-	-	-	R	R	R	R
Name	IIC_FIFO_TX_EMPTY	Reserved			IIC_FIFO_TX_INDEX[3:0]			

Bit Number	Bit Mnemonic	Description
7	IIC_FIFO_TX_EMPTY	I²C transmit FIFO clear flag
6-4	Reserved	-
3-0	IIC_FIFO_TX_INDEX[3:0]	I²C transmit FIFO index

-: unimplemented.

Slave I²C RX FIFO Control Register I²C_RXFIFO_INDEX (XFR: 0xAA) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	-	-	-	R	R	R	R
Name	IIC_FIFO_RX_FULL	Reserved			IIC_FIFO_RX_INDEX[3:0]			

Bit Number	Bit Mnemonic	Description
7	IIC_FIFO_RX_FULL	I²C receive FIFO full flag
6-4	Reserved	-
3-0	IIC_FIFO_RX_INDEX[3:0]	I²C FIFO index value

-: unimplemented.

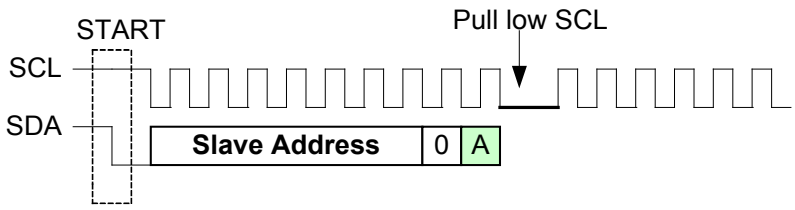
Slave I²C Transmit Receive Buffer Data Register I²C_BUFF (XFR: 0xAB) **Reset Value: FFh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IIC_FIFO_DAT[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	IIC_FIFO_DAT[7:0]	R: Read data from RX FIFO W: Write data into TX FIFO

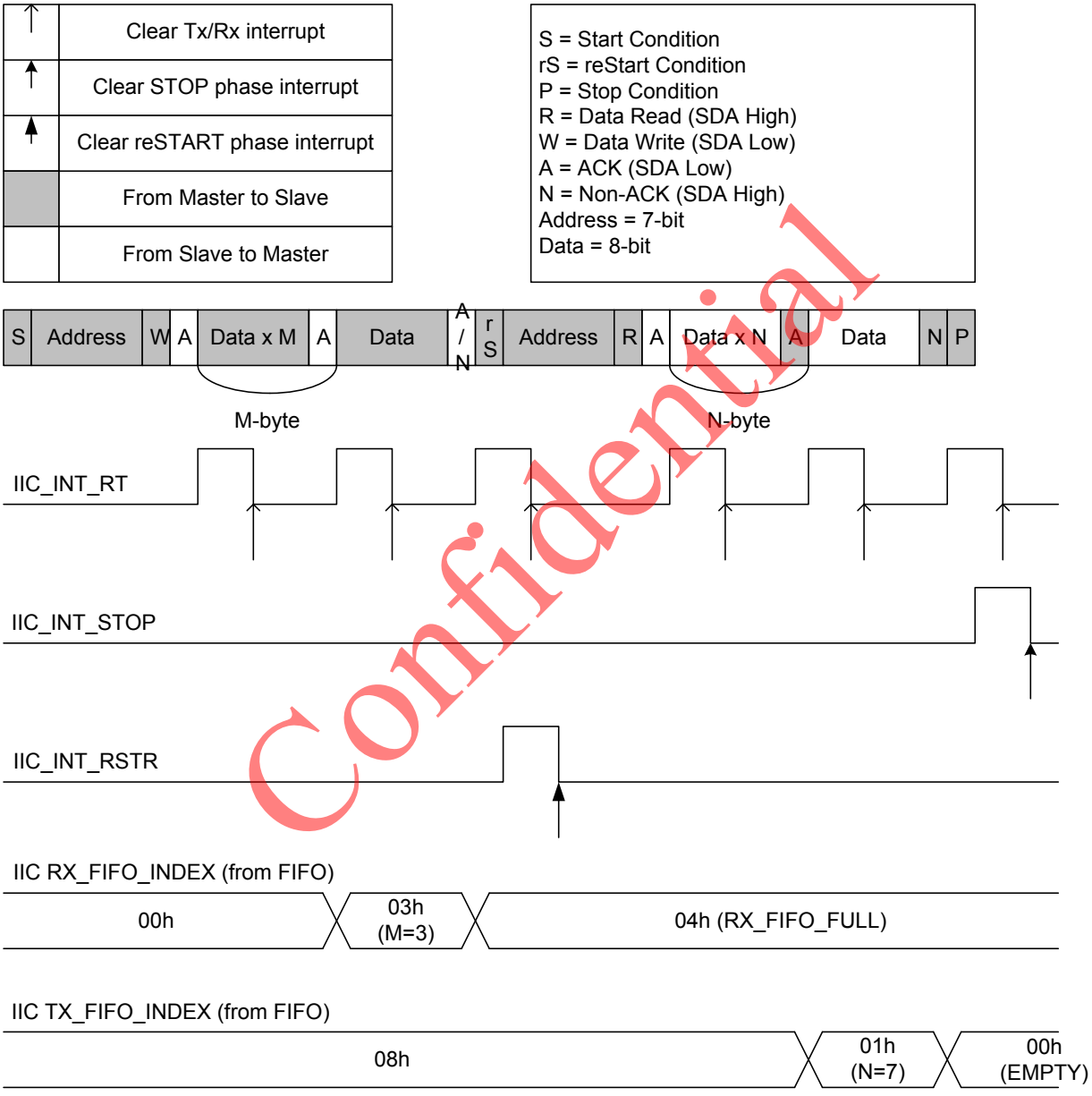
-: unimplemented.

If the firmware takes longer to process than I²C receiving 9 bits, the firmware have to set MI²C_WAIT, enabling WT51F516 pull low SCL at the 9th bit and let the master wait for it.



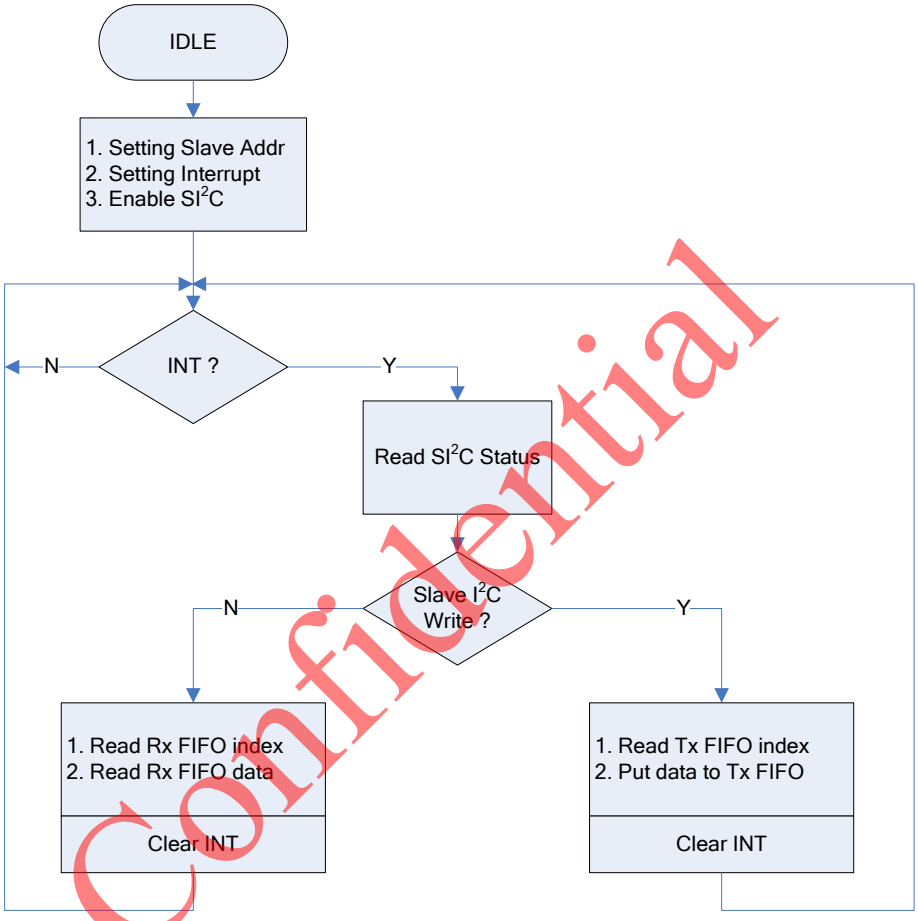
WT51F516 Slave I²C Interrupt Timing

WT51F516 Slave I²C with 8-FIFO Interrupt Timing



WT51F516 Slave I²C Flow Chart

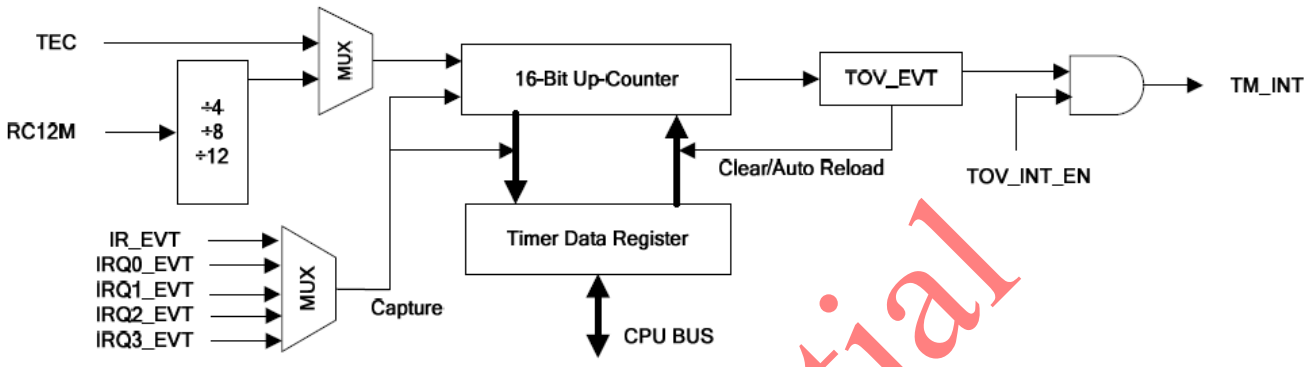
WT51F516 Slave I²C with 8-FIFO Flow Chart



6.14 Enhanced Timer/Counter

The clock sources of enhanced Timer/Counter are from internal or external clock, and it is determined by register.

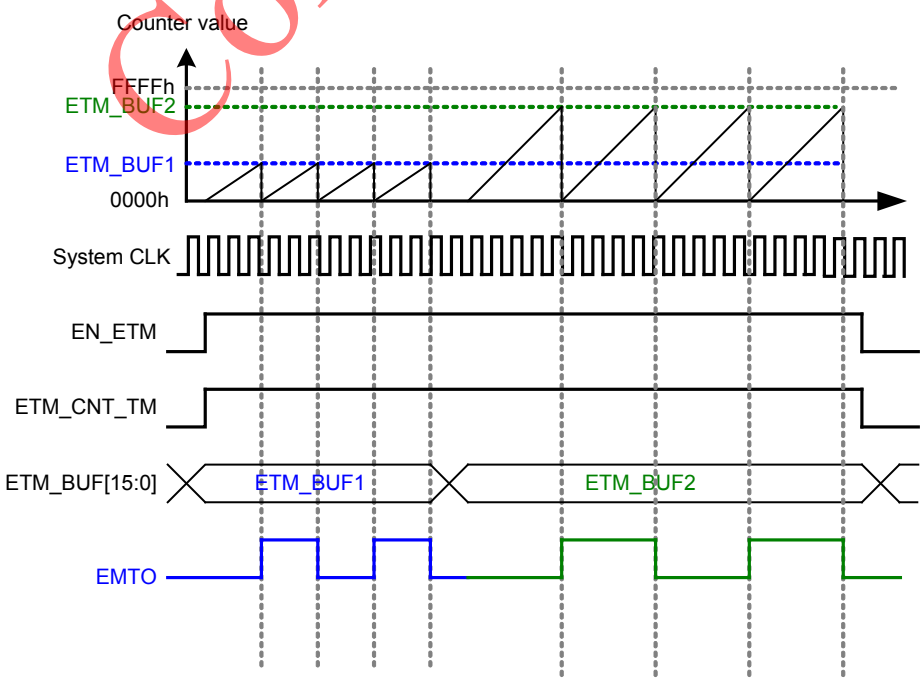
The Enhanced Timer/Counter has two operation modes: 1. Compare mode. 2. Capture mode. and there are three types of Capture Match condition for selection: High-level, Low-level, and Period of Capture mode.



1. Compare Mode

The Enhanced Timer/Counter contains one 16-bit Counter and one 16-bit enhanced Buffer (TCDR[15:0]). When enable the Enhanced Timer/Counter (TC_EN = 1) and set as the compare mode (CAP_RL_SEL = 0), the timer will start counting according to the clock sources, and an interrupt will occur once the data of the counter matches the data of the enhanced Buffer. Each match will trigger the interrupt and clear the counter value of the internal 16-bit Counter. Please refer to the figure below.

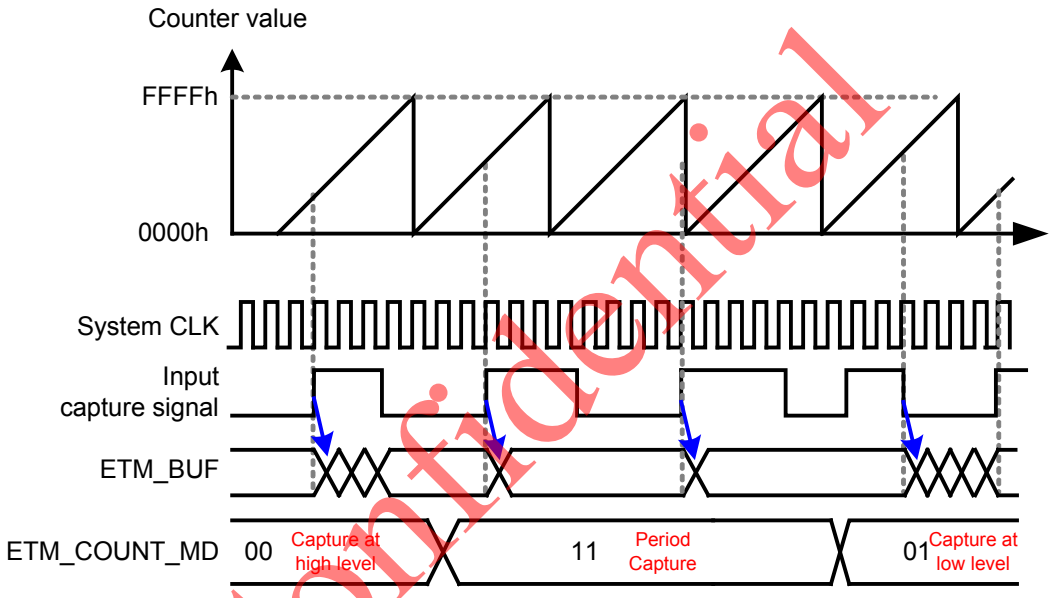
Compare mode operation flow:



2. Capture mode

If the Enhanced Timer/Counter is set as the Capture mode (CAP_RL_SEL = 1), and it is enabled (TC_EN = 1), the capture operation starts. When the input status changes then match with the setting capture condition, the internal 16-bit counter will be cleared and restarts counting, then reload the counter value into 16-bit Buffer (TCDR[15:0]) automatically. At the same time, the software can read the counter value from the Enhanced Timer/Counter Data Buffer Register (register 82H & 83H), and then a capture interrupt and capture flag may be generated simultaneously. Please refer to the figure below.

Capture mode operation flow:



Enhanced Timer/Counter Control Register 1 ETM_CTL1 (XFR: 0x80) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	TC_EN	EXC_EN	TCC_SEL[1:0]		CAP_RL_SEL	CAP_SEL[2:0]		

Bit Number	Bit Mnemonic	Description
7	TC_EN	1: Enable Enhanced Timer/Counter
6	EXC_EN	Set clock source of Enhanced Timer/Counter 1: external clock source (can select the input clock source by TEC (GPIOA0) 0: internal clock source (SOURCE clock)
5-4	TCC_SEL[1:0]	Set clock source prescalers of the internal 16-bit Counter 00: Enhanced Timer/Counter clock source = SOURCE clock 01: Enhanced Timer/Counter clock source = SOURCE clock / 4 10: Enhanced Timer/Counter clock source = SOURCE clock / 8 11: Enhanced Timer/Counter clock source = SOURCE clock / 12
3	CAP_RL_SEL	1: Capture mode 0: Compare mode (SOURCE clock = 12 MHz)

Bit Number	Bit Mnemonic	Description
2-0	CAP_SEL[2:0]	Set Enhanced Timer/Counter input external clock source channel = 1XX, IR edge triggered = 000, IRQ0 triggered = 001, IRQ1 triggered = 010, IRQ2 triggered = 011, IRQ3 triggered

-: unimplemented.

Enhanced Timer/Counter Control Register 2 ETM_CTL2 (XFR: 0x81) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	-	-	-	R/W	-	-	-
Name	TCOV_INT_EN	Reserved			ETM_IN_PSCAL[1:0]	Reserved		

Bit Number	Bit Mnemonic	Description
7	TCOV_INT_EN	1: Enable overflow flag
6-4	Reserved	-
3	TCOV_EVT(1)	Overflow flag 1: When an overflow occurred in internal 16-bit counter, TCOV_EVT = 1
2-0	Reserved	-

-: unimplemented.

Enhanced Timer/Counter Data Buffer High Bytes Register ETM_BUF[15:8] (XFR: 0x82) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	TCDR[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	TCDR [15:8]	Paired with ETM_BUF[7:0] to form a 16-bit counter value Read: In Capture mode, the counter value of the captured input signal Write: In Compare mode, as the compare value to compare with the internal 16-bit counter

Enhanced Timer/Counter Data Buffer Low Bytes Register ETM_BUF[7:0] (XFR: 0x83) Reset Value: 00h

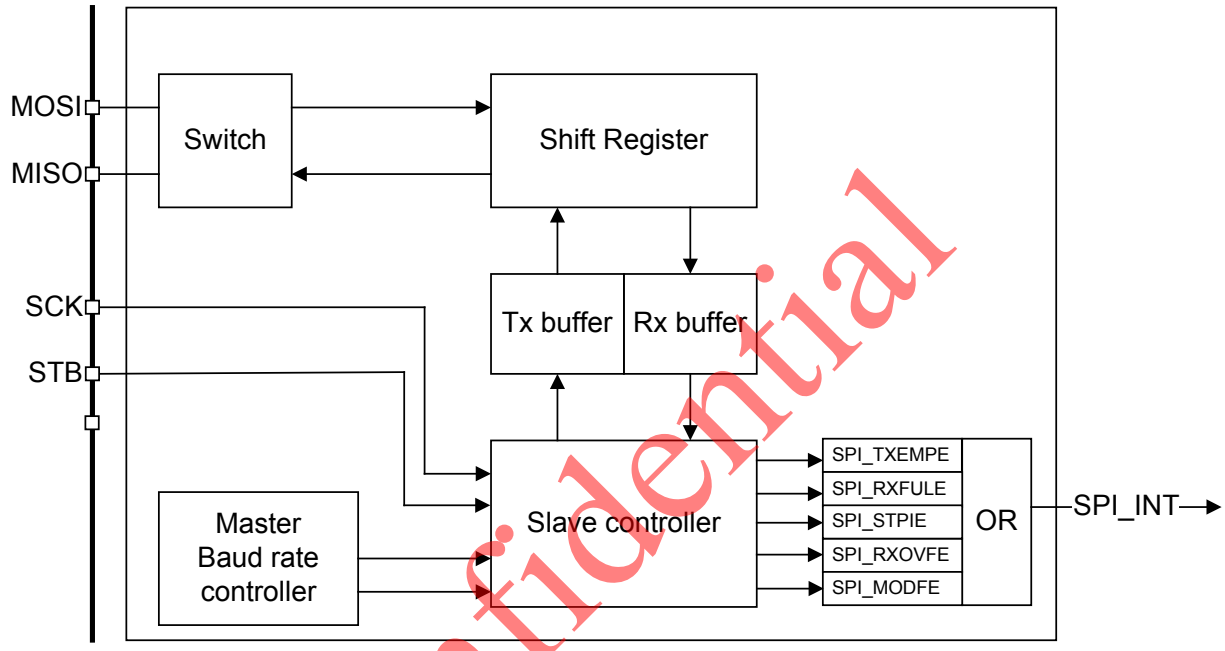
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	TCDR[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	TCDR [7:0]	Paired with ETM_BUF[15:8] to form a 16-bit counter value Read: In Capture mode, the counter value of the captured input signal Write: In Compare mode, as the compare value to compare with the internal 16-bit counter

6.15 Serial Peripheral Interface (SPI)

SPI is a synchronous serial interface, allows master to communicate with slave, supports full duplex data transmission, and also supports 3-wire or 4-wire communication.

- SPI supports: Master and Slave mode
- Transmitted serial data can select LSB or MSB being transmitted first
- SPI serial interface transmission speed, frequency range: 2 MHz ~ 23.4375 kHz (Bit Rate)



SPI communication uses four pins, as described below.

MOSI: In Master mode data output; in Slave mode data input.

MISO: In Master mode data input; in Slave mode data output.

SCK: In Master mode clock output; in Slave mode clock input for data synchronization.

STB: In Master mode as output; in Slave mode as input.

In Master mode, as the I/O port to enable Slave:

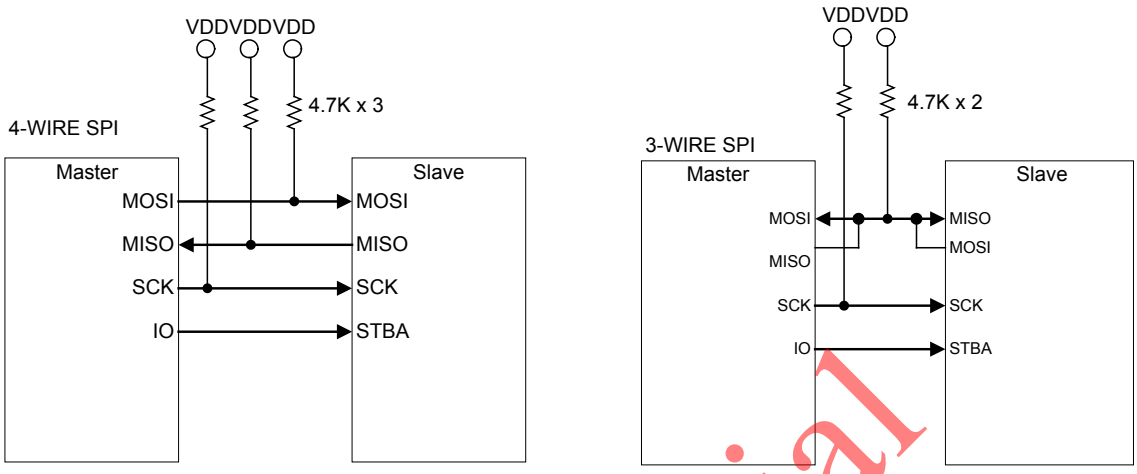
STB = 0: Master enables Slave

STB = 1: Master disables Slave

When use the SPI serial interface, the SPI related pins must be set as output or input status by software, as illustrated below:

4-wire SPI	Master mode	Slave mode	Remarks
MOSI (GPIOA5)	Output	Input	
MISO (GPIOC6)	Input	Output	
SCK (GPIOC7)	Output	Input	
STB (GPIOA4)	Output	Input	

4-wire and 3-wire SPI connection diagram:



SPI Control Register 1 SPI_CTL1 (XFR: 0xC0) **Reset Value: 0x00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	SPI_EN	SPI_MASTER	SPI_CPOL	SPI_CPHA	SPI_MODFEN	SPI_LSBFE	SPI_SPC	SPI_BIDIROE

Bit Number	Bit Mnemonic	Description
7	SPI_EN	1: Enable SPI module 0: Disable SPI module
6	SPI_MASTER	SPI Master/Slave mode selection 1: SPI as Master mode 0: SPI as Slave mode
5	SPI_CPOL	SPI Clock Polarity bit selection 1: Active-low clock selection 0: Active-high clock selection
4	SPI_CPHA	SPI Clock Phase bit selection 1: sampling data at even edge of input SPI clock 0: sampling data at odd edge of input SPI clock
3	SPI_MODFEN	1: Enable SPI failure mode (Slave mode use only) 0: Disable SPI failure mode (Slave mode use only)
2	SPI_LSBFE	LSB-First Enable 1: Data is transferred LSB bit first 0: Data is transferred MSB bit first
1	SPI_SPC	SPI Serial pin control setting (3-wire) 1: Enable SPI bidirectional transmission setting 0: Disable SPI bidirectional transmission setting
0	SPI_BIDIROE	Valid only when SPI_SPC = 1 (3-wire) 1: Slave: MISO as Output (MOSI is invalid in Slave mode) Master: MOSI as Output (MISO is invalid in Master mode) 0: Slave: MISO as Input (MOSI is invalid in Slave mode) Master: MOSI as Input (MISO is invalid in Master mode)

Note:

Mode	Register SPI_CTL1[1]	Register SPI_CTL1[0]	MISO pin status	MOSI pin status
Pin Mode	SPC0	BIDIROE	MISO	MOSI
Operates in Master mode				
Normal	0	X	Master input	Master output
Bidirectional	1	0	MISO invalid	Master input
		1		Master input/output
Operates in Slave mode				
Normal	0	X	Slave output	Slave In
Bidirectional	1	0	Slave input	MOSI invalid
		1	Slave input/output	

SPI Interrupt Control Register SPI_INT (XFR: 0xC1) **Reset Value: 0x00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Name	SPI_TXIE	SPI_RXIE	SPI_STPIE	Reserved	TX_INT_NUM[1:0]		RX_INT_NUM[1:0]	

Bit Number	Bit Mnemonic	Description
7	SPI_TXIE	1: Enable SPI Tx data buffer interrupt
6	SPI_RXIE	1: Enable SPI Rx data buffer interrupt
5	SPI_STPIE	1: Enable SPI Transmission sequence finish interrupt
4	Reserved	-
3-2	TX_INT_NUM[1:0]	Set the interrupt occurred at transmitting every n bytes 00: 1-byte interrupt 01: 2-byte interrupt 10: 4-byte interrupt 11: 8-byte interrupt
1-0	RX_INT_NUM[1:0]	Set the interrupt occurred at receiving every n bytes 00: 1-byte interrupt 01: 2-byte interrupt 10: 4-byte interrupt 11: 8-byte interrupt

-: unimplemented.

SPI Interrupt Clear Register SPI_CLR (XFR: 0xC2) **Reset Value: 0x00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	-	-	-	-	-
Name	CLR_TXIF	CLR_RXIF	CLR_STPIF	Reserved				

Bit Number	Bit Mnemonic	Description
7	CLR_TXIF	1: Clear SPI Tx interrupt flag
6	CLR_RXIF	1: Clear SPI Rx interrupt flag
5	CLR_STPIF	1: Clear SPI sequence finish interrupt flag
4-0	Reserved	-

-: unimplemented.

SPI Flag Register SPI_FLG (XFR: 0xC3) **Reset Value: 0x00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	-	-	-	-
Name	SPI_TXIF	SPI_RXIF	SPI_STPIF	SPI_MODF	Reserved			

Bit Number	Bit Mnemonic	Description
7	SPI_TXIF	SPI transmit data buffer status flag *1 1: SPI Tx data buffer is finished
6	SPI_RXIF	SPI receive data buffer status flag 1: SPI Rx data buffer is finished
5	SPI_STPIF	SPI transmit/receive data finish status flag (SS pin go high) 1: SPI Tx/Rx data is finished
4	SPI_MODF	SPI mode failure status flag (Slave mode only) *3 1: SPI mode failure
3-0	Reserved	-

-: unimplemented.

SPI Bit Rate Setting Register SPI_BRS[7:0] (XFR: 0xC4) **Reset Value: 0x00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	SPI_BRS[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	SPI_BRS[7:0]	SPI Bit rate selection (SPI maximum = 2M) SPI Bit Rate = SCLK / (SPI_BRS[7:0]+1) x 2 If mcu_clk = 12 MHz BRS[7:0]=0: SPI speed = 12 MHz/(255+1) x 2 = 23.4375 kHz BRS[7:0]=1: SPI speed = 12 MHz/(255+1) x 2 = 23.4375 kHz BRS[7:0]=2: SPI speed = 12 MHz/(2+1) x 2 = 2 MHz BRS[7:0]=3: SPI speed = 12 MHz/(3+1) x 2 = 1.5 MHz . . . BRS[7:0]=0: SPI speed = 12 MHz/(255+1)x2 = 23.4375 kHz

SPI FIFO Control Register SPI_FIFO (XFR: 0xC8) **Reset Value: 0x00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	-	-	-	-	-	-
Name	CLR_SPI_TXFIFO_INDEX	CLR_SPI_RXFIFO_INDEX	Reserved					

Bit Number	Bit Mnemonic	Description
7	CLR_SPI_TXFIFO_INDEX	1: Clear SPI Transmit data buffer index
6	CLR_SPI_RXFIFO_INDEX	1: Clear SPI Receive data buffer index
5-0	Reserved	-

-: unimplemented.

SPI FIFO Transmit Status Register SPI_TX_FIFO (XFR: 0xC9) **Reset Value: 0x80h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	-	-	-	R	R	R	R
Name	SPI_FIFO_TX_EMPTY	Reserved			SPI_FIFO_TX_INDEX[3:0]			

Bit Number	Bit Mnemonic	Description
7	SPI_FIFO_TX_EMPTY	SPI Transmit Data Buffer Empty flag*1 1: SPI Tx data buffer is empty
6-4	Reserved	-
3-0	SPI_FIFO_TX_INDEX[3:0]	SPI Tx data buffer index

-: unimplemented.

SPI FIFO Receive Status Register SPI_RX_FIFO (XFR: 0xCA) **Reset Value: 0x00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	-	-	-	R	R	R	R
Name	SPI_FIFO_RX_FULL	Reserved			SPI_FIFO_RX_INDEX[3:0]			

Bit Number	Bit Mnemonic	Description
7	SPI_FIFO_RX_FULL	SPI receive data buffer full flag 1: SPI receive buffer is full
6-4	Reserved	-
3-0	SPI_FIFO_TX_INDEX[3:0]	SPI Rx data buffer index

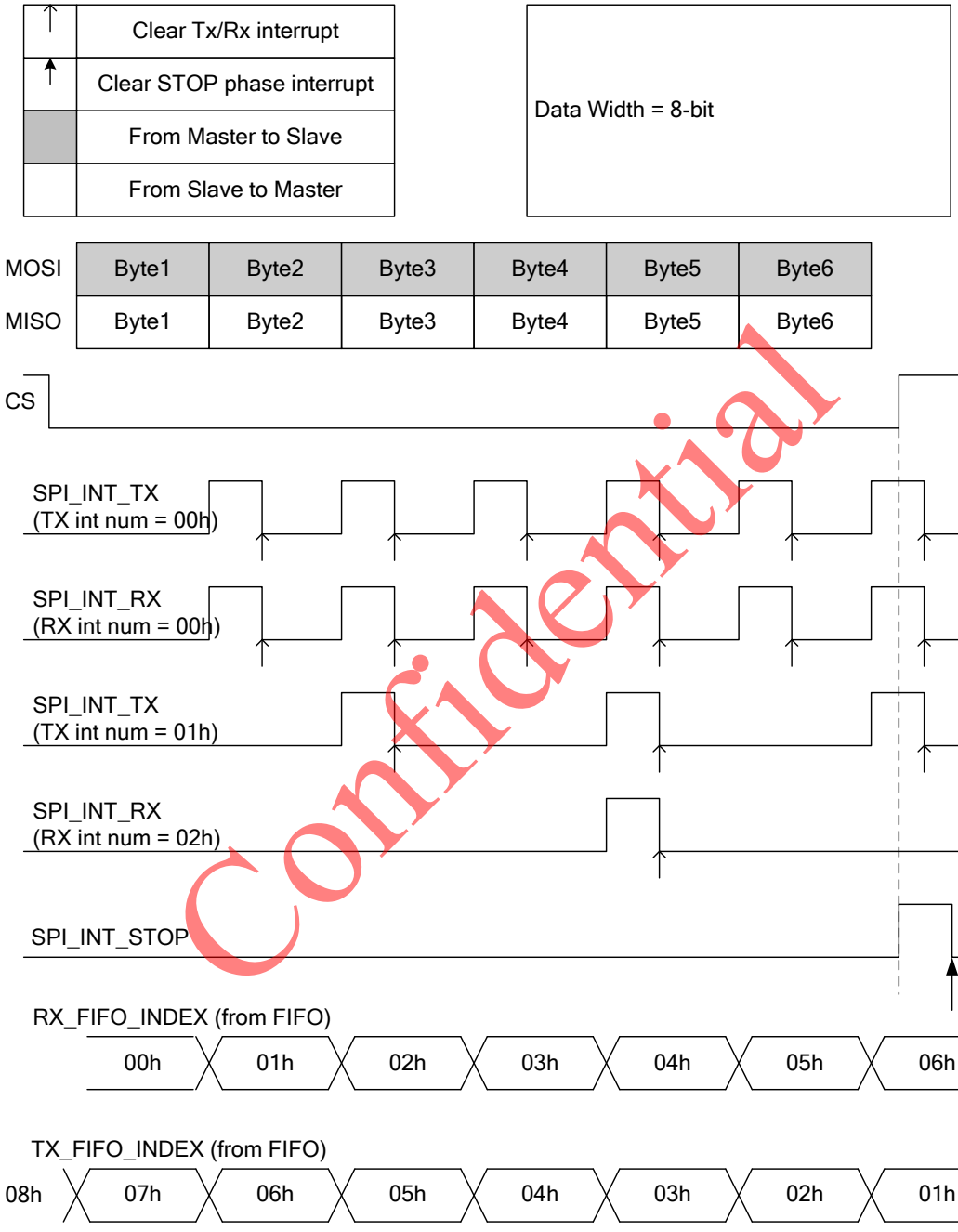
-: unimplemented.

SPI Transmit Receive Buffer Register SPI_DAT[7:0] (XFR: 0xCB) **Reset Value: 0xFFh**

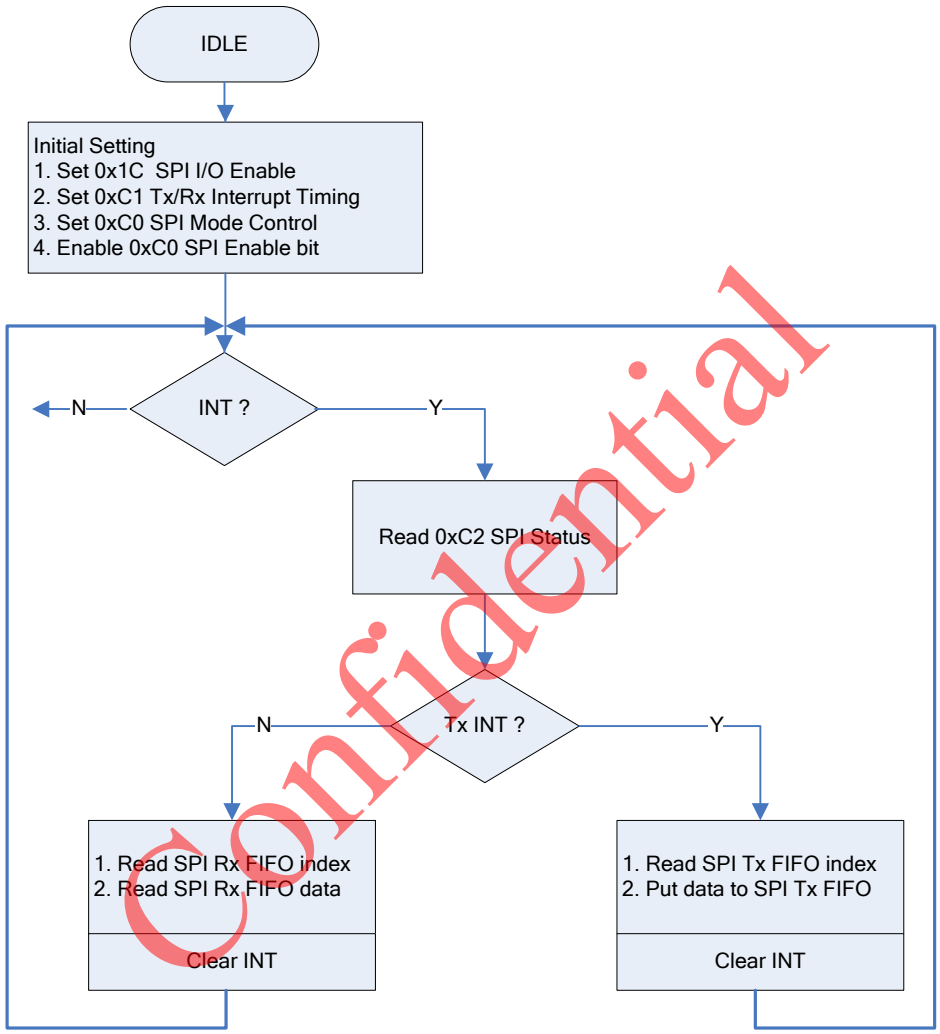
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	FIFO_DAT[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	FIFO_DAT[7:0]	Read: Read data from SPI RX FIFO Write: Write data into SPI TX FIFO

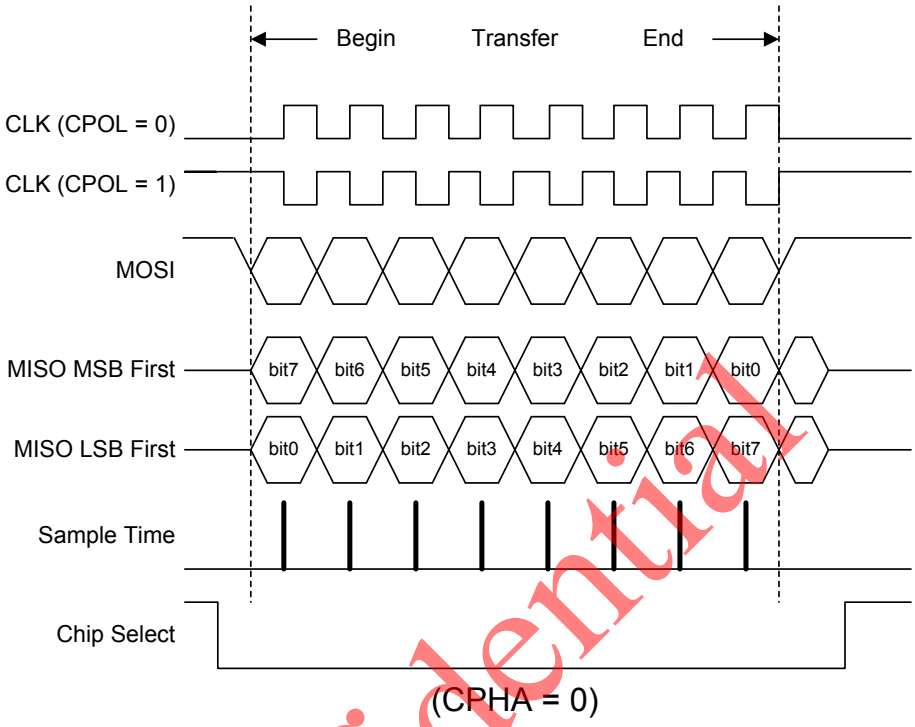
WT51F516 SPI with 8-FIFO Interrupt Timing



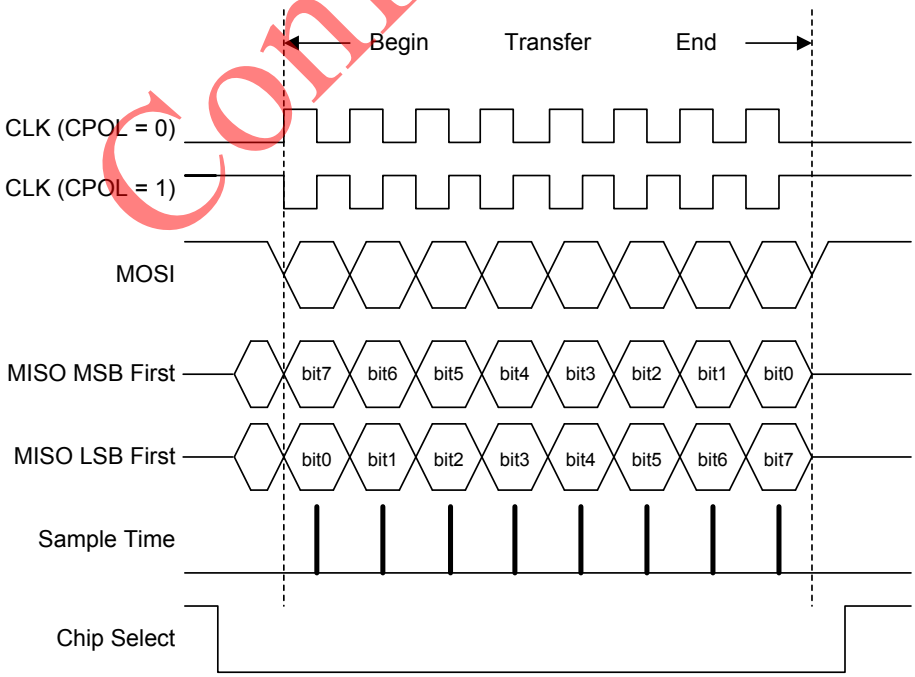
WT51F516 M/S SPI with 8-FIFO Flow Chart



Transmit and Receive methods can refer to "SPI Mode Timing"



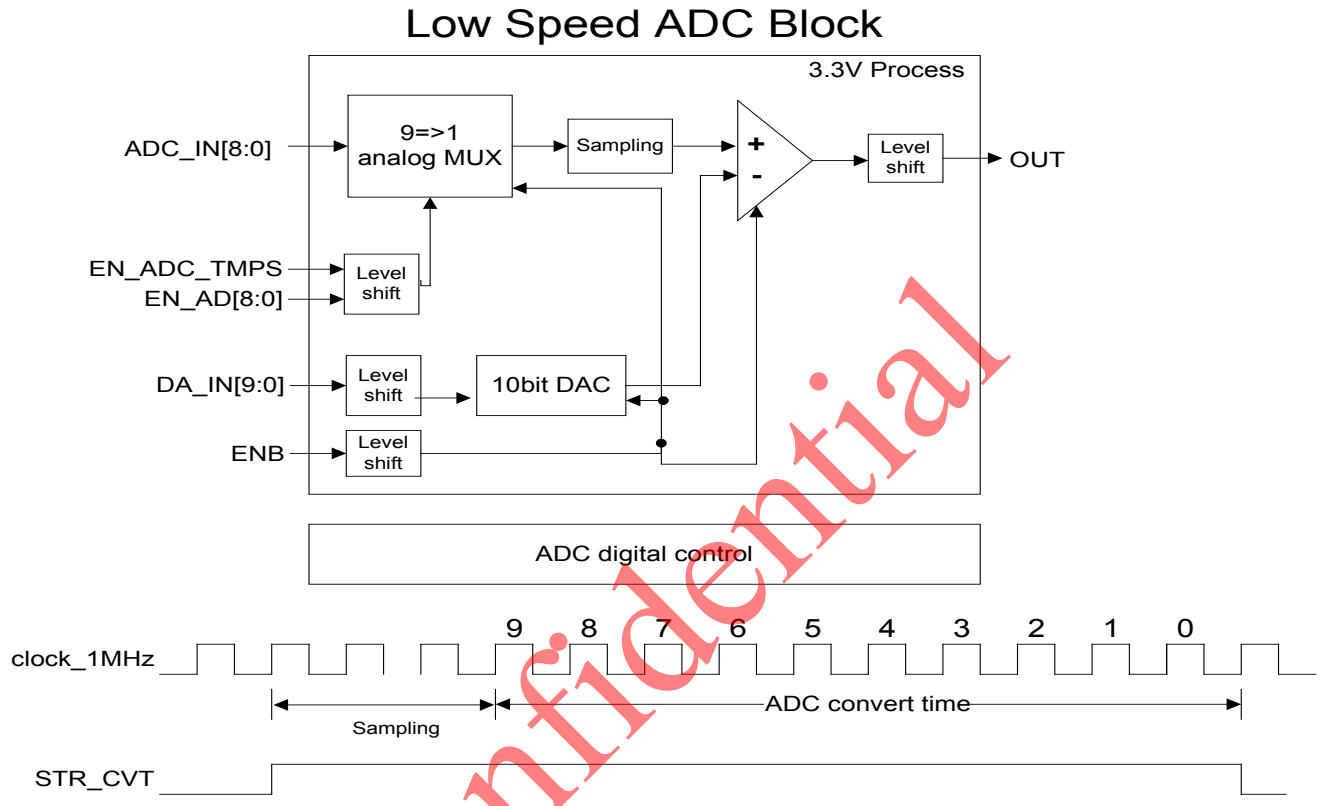
(CPHA = 0)



(CPHA = 1)

6.16 Analog/Digital Converter (ADC)

WT51F516 has a built-in 8-channel 10-bit Analog/Digital Converter, and it also provides two conversion modes (Single, and Voltage Compare) and four conversion rate (1 MHz, 250 kHz, 62.5 kHz, 15.625 kHz) for selection.



Single Mode:

Turn on the A/D converter power (ADC Control Register, and PD_LADC = 0), and set the STR_CVT = 1, then the A/D conversion starts. When STR_CVT = 0, the conversion is finished, and it takes 16us in each channel conversion.

Voltage Compare Mode:

When turn on the A/D converter power (ADC Control Register, and PD_LADC = 0), and activate the Compare function (EN_ADC_WK = 1), it is allowed to proceed AD conversion of the Analog (ADC_IN) and compare it with the Voltage Compare Data Register (ADC_WK_V). When the corresponding digital value of the voltage analog input is greater than (ADC_BIG = 0) or smaller than (ADC_BIG = 1) the setting value of ADC Voltage Compare Data Register (ADC_WK_V), the ADC interrupt will occur. The Voltage Compare function of A/D Converter module as a wakeup source.

ADC Control Register ADC_CTL (XFR: 0xD0) **Reset Value: 0x80h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PD_LADC	STR_CVT	ADC_BIG	EN_ADC_WK	SLT_FLT_CVT	RDNOISE	ADC_CLK_SEL	

Bit Number	Bit Mnemonic	Description
7	PD_LADC	Analog/Digital Converter Power Control 1: turn off ADC power 0: turn on ADC power
6	STR_CVT	ADC start convert bit (single convert mode) 1: ADC start convert 1 => 0: convert finished (hardware will be auto-cleared as"0")
5	ADC_BIG	ADC data compare flag 1: the data set when Vin < ADC_CMP_V[9:0] 0: the data set when Vin > ADC_WK_V[9:0] Vin: the channel selected by EN_AD[3:0]
4	EN_ADC_WK	1: turn on ADC wakeup mode 0: turn off ADC wakeup mode
3	SLT_FLT_CVT	1: turn on 250ns filter convert data 0: turn off filter
2	RDNOISE	1: reduce noise when ADC convert (halt 8052 clock 16 us) 0: didn't reduce noise when ADC convert
1-0	ADC_CLK_SEL	ADC convert frequency selection 00: 1 MHz 01: 250 kHz 10: 62.5 kHz 11: 15.625 kHz

ADC Converted Data High Bytes Register AD_DATA[9:2] (XFR: 0xD1) Reset Value: 0x00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	AD_DATA[9:2]							

Bit Number	Bit Mnemonic	Description
7-0	AD_DATA[9:2]	AD_DATA[9:2] converted data setting, paired with AD_DATA[1:0] to form a 10-bit data

ADC Voltage Compare Wakeup Data High Bytes Register ADC_WK_V[9:2] (XFR: 0xD2) Reset Value: 0x80h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	ADC_WK_V[9:2]							

Bit Number	Bit Mnemonic	Description
7-0	ADC_WK_V[9:2]	ADC_WK_V[9:2] compare setting, paired with ADC_WK_V[1:0] to form a 10-bit data

ADC Channel Control Register ADC_ENCH (XFR: 0xD3) Reset Value: 0x00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	EN_AD[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	EN_AD[7:0]	Analog/Digital Channel selection 0000: select channel CH0 0001: select channel CH1 0010: select channel CH2 0011: select channel CH3 0100: select channel CH4 0101: select channel CH5 0110: select channel CH6 0111: select channel CH7

ADC Converted Data Low Bytes Register AD_DATA[1:0] (XFR: 0xD4) Reset Value: 0x00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R	R
Name	Reserved						AD_DATA[1:0]	

Bit Number	Bit Mnemonic	Description
7-2	Reserved	-
1-0	AD_DATA[1:0]	AD_DATA[1:0] converted data setting, paired with AD_DATA[9:2] to form a 10-bit data

-: unimplemented.

ADC Voltage Compare Wakeup Data Low Bytes Register ADC_WK_V[1:0] (XFR: 0xD5) Reset Value: 0x00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved						ADC_WK_V[1:0]	

Bit Number	Bit Mnemonic	Description
7-2	Reserved	-
1-0	ADC_WK_V[1:0]	ADC_WK_V[1:0] compare setting, paired with ADC_WK_V[9:2] to form a 10-bit data

-: unimplemented.

ADC Temperature Sensor Control Register EN_ADC_TMPS (XFR: 0xD6) Reset Value: 0x00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	-	R/W
Name	Reserved							EN_ADC_TMPS

Bit Number	Bit Mnemonic	Description
7-1	Reserved	-
0	EN_ADC_TMPS	1: turn on the gate of ADC to temperature sensor transmission 0: turn off the gate of ADC to temperature sensor transmission

-: unimplemented.

ADC Setting Control Register ADC_SEL (XFR: 0xD7) **Reset Value: 0x04h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	R/W	R/W	R/W
Name	Reserved					VREF_SEL[2:0]		

Bit Number	Bit Mnemonic	Description
7-3	Reserved	-
2-0	VREF_SEL[2:0]	ADC reference voltage selection 100: from AVDD 010: from AREF pin 001: from internal reference voltage 1.262V (must turn off PD_TMPS, D8H-bit7) others: not available

-: unimplemented.

Note:

(a) Reading register "D1h" to clear ADC wakeup interrupt flag

(b) EN_AD[7:0] & EN_ADC_TMPS can only enable one channel at the same time

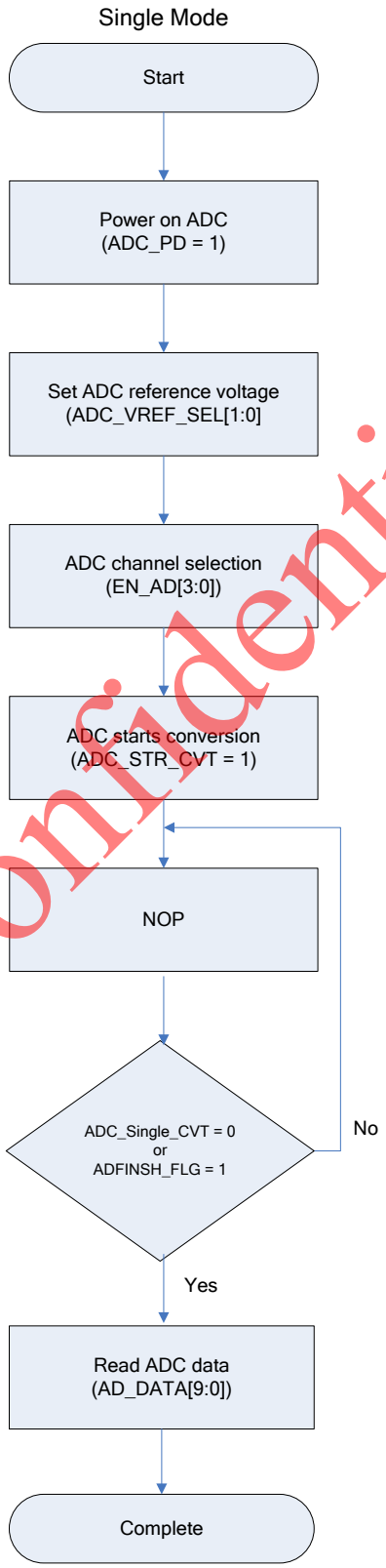
(c) When converting temperature sensor voltage, please set ADC_CLK_SET = 10 or 11

(d) Offset voltage value are stored in Flash memory XDATA 0xFFCH-bit[7:0], and the sampled calibration value VREF_D[7:0] (VREF 3.3V 10-Bit ADC) are stored in this address. The last 8-bit LSB code is stored in XDATA 0xFFCH-bit[7:0] to calibrate temperature sensor, and the first 2-bit MSB is 3h.

For example, XDATA 0xFFCH = 2BH, the fully VREF_D code is 32BH,

Internal reference voltage = $\frac{1024}{VREF\_D}$ **=** $\frac{1024}{32BH}$ **= 1.263v**

The setting of Enabling Analog/Digital Converter converted Data procedure:



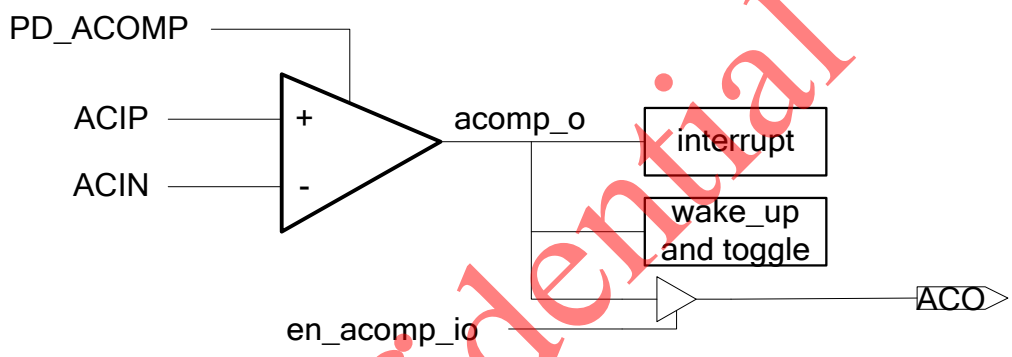
6.17 Comparator

WT51F516 built-in one Analog Voltage Comparator with features as listed below.

- Comparator can be enabled or disabled individually.
- Either the positive-edge or negative-edge of the comparator can generate Interrupt.

When the comparator function is enabled (XFR: 0xD9, Control Register ACOMP_CTL, ACOMP_PD = 0), the comparator can compare input with analog ACIP and ACIN. The three methods of performing are listed below:

1. Interrupt
2. Wakeup
3. Event output (ACO)



Comparator Control Register ACOMP_CTL (XFR: 0xD9) **Reset Value: 0x80h**

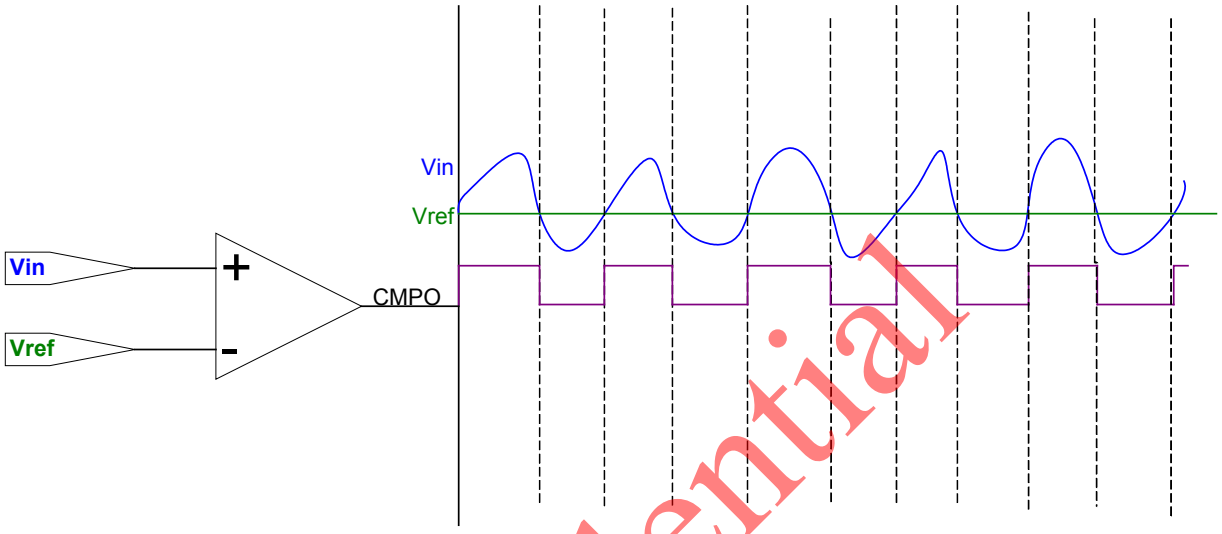
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	-	R/W	-	-	-
Name	ACOMP_PD	ACOMP_EDGE	CLR_ACOMP_EVENT	Reserved	ACOMP_EVENT	Reserved		

Bit Number	Bit Mnemonic	Description
7	ACOMP_PD	1: Power down Comparator 0: Power on Comparator
6	ACOMP_EDGE	1: if ACIP voltage > ACIN voltage, then ACOMP_EVENT = 1 0: if ACIP voltage < ACIN voltage, then ACOMP_EVENT = 1
5	CLR_ACOMP_EVENT	1: Clear comparator flag
4	Reserved	-
3	ACOMP_EVENT	1: comparator flag 0: if ACOMP_PD = 1, then ACOMP_EVENT = 0
2-0	Reserved	-

-: unimplemented.

(1) After enabling ACOMP, the voltage is unstable, thus setting CLR_ACOMP_EVENT clear flag bit is necessary.

Example: The figure below shows comparator input via the enhanced timer to perform Gating Timer to capture low-level or high-level period.



6.18 Low Voltage Detection (LVD)

WT51F516 has a built-in Low Voltage Detection circuitry which can detect the supply voltage falls below the minimum specified operating voltage then generates an Interrupt.

- The Enable and Disable function of Low Voltage Detection are controlled by the software
- Low Voltage Detection level provides four levels of voltage for selection: 2.50V, 3.00V, 3.50V or 4V

Low Voltage Detection Control Register LVD_CTL (XFR: 0x0B) **Reset Value: 80H**

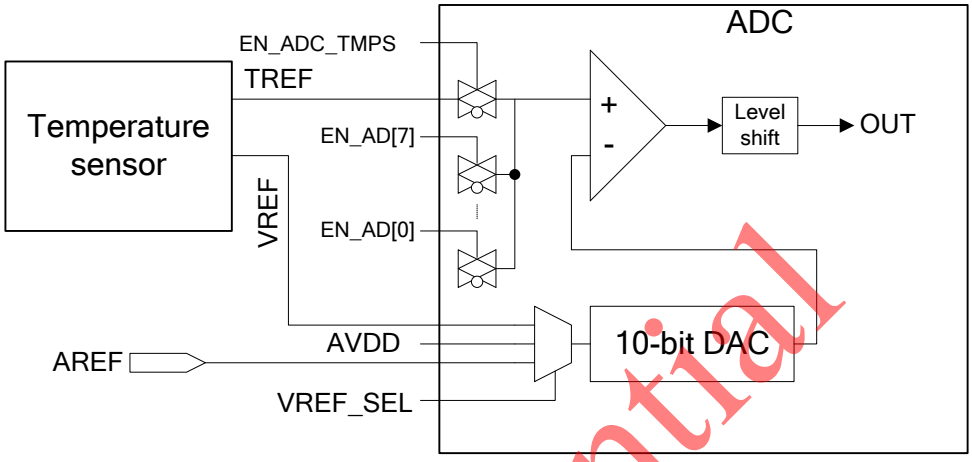
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	-	-	-	-	R/W	R/W	-
Name	LVD_PD	Reserved				LVD_SEL[1:0]		Reserved

Bit Number	Bit Mnemonic	Description
7	LVD_PD	1: Power down Low Voltage Detection 0: Power on Low Voltage Detection
6-3	Reserved	-
2-1	LVD_SEL[1:0]	Low Voltage Detection range: 00: < 2.5V 01: < 3V 10: < 3.5V 11: < 4V
0	Reserved	-

-: unimplemented.

6.19 Temperature Sensor

Temperature Sensor can be used in large-scale industry or small-scale home appliances. Temperature Sensor components can read 10-bit ADC value, and convert the ambient temperature of MCU by formula.



Temperature Sensor Setting Control Register TS_SEL (XFR: 0xD8) Reset Value: 0x80h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	-	-	-	-	-	R/W	R/W
Name	PD_TMPS	Reserved					TMPS_GAIN[1:0]	

Bit Number	Bit Mnemonic	Description
7	PD_TMPS	1: Disable temperature sensor (default) 0: Enable temperature sensor
6-2	Reserved	-
1-0	TMPS_GAIN[1:0]	Amplifier control selection 00: 0.9486~0.5600V (388.6mV) 01: 1.5777~0.9338V (643.9mV) 10: 2.2070~1.3040V (903.0mV) 11: 2.8377~1.6783V (1159.4mV)

-: unimplemented.

Converting methods:

(a) Temperature Sensor offset voltage value are stored in Flash memory XDATA 0xFFDH-bit[7:0]. After production, the temperature sensor calibration value TS_TREF_D[7:0] sampled in room temperature by VREF 3.3V 10-Bit ADC will be stored in this address, the last 8-bit LSB is stored in XDATA 0xFFDH-bit[7:0] to calibrate Temperature Sensor. The first 2-bit MSB is 2h, and the ideal code in room temperature is 2E7H.

For example: XDATA 0xFFDH = DFH, and the fully TREF_D code is 2DFH.

$$Calibrated\_Temp = \frac{(2E7H - 2DFH) * 3.223mV}{-0.0066} = -3.9067\,℃$$

TMPS_GAIN	Temp.(℃) - Equation	Note
00	$\frac{TS\_TREF\_Voltage - 0.85}{-0.00213} + Calibrated\_Temp$	ADC Verve > 1.2V
01	$\frac{TS\_TREF\_Voltage - 1.42}{-0.00375} + Calibrated\_Temp$	ADC Verve > 1.8V
10	$\frac{TS\_TREF\_Voltage - 1.98}{-0.0052} + Calibrated\_Temp$	ADC Verve > 2.4V
11	$\frac{TS\_TREF\_Voltage - 2.55}{-0.0066} + Calibrated\_Temp$	ADC Verve > 3.0V

TS_TREF voltage is the voltage value read by ADC converting result.

For example: ADC VREF = 3.3V, and TMPS_GAIN = 11, if the ADC code is 2AAH and TREF_D[7:0] = DFH

TS_TREF Voltage= $\frac{AD\_DATA}{1024} * ADC\_VREF = \frac{2AAH}{1024} * 3.3v$ = 2.198V

$$Temperature = \frac{TS\_TREF\_Voltage - 2.55}{-0.0066} + Calibrated\_Temp = \frac{2.198 - 2.55}{-0.0066} + (-3.9067) = 49.43\ ℃$$

***The tolerance of sampled calibration value in room temperature is about 25℃ ±3℃.**

6.20 Emulated E²PROM

The WT51F516 can use Flash PROM space to emulate E²PROM, and the storage address ranges from: 0x3000 ~ 0x3FF0.

E²PROM Enable Register 1 EER_EN1[3:0] (XFR: 0xE0) **Reset Value: 0x00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	W	W	W	W
Name	Reserved				EER_EN1[3:0]			

Bit Number	Bit Mnemonic	Description
7-4	Reserved	-
3-0	EER_EN1[3:0]	When EER_EN1[3:0] = '1010' and EER_EN2[3:0] = '0101', the E²PROM function is enabled.

-: unimplemented.

E²PROM Enable Register 2 EER_EN2[3:0] (XFR: 0xE1) **Reset Value: 0x00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	W	W	W	W
Name	Reserved				EER_EN2[3:0]			

Bit Number	Bit Mnemonic	Description
7-4	Reserved	-
3-0	EER_EN2[3:0]	When EER_EN2[3:0] = '0101' and EER_EN1[3:0] = '1010', the E²PROM function is enabled

-: unimplemented.

E²PROM Address Low Bytes Register EER_ADDR[7:0] (XFR: 0xE2) **Reset Value: 0xFFh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	EER_ADDR[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	EER_ADDR[7:0]	EER_ADDR[7:0] address setting, paired with EER_ADDR[11:8] to form a 12-bit address

E²PROM Address High Bytes Register EER_ADDR[11:8] (XFR: 0xE3) **Reset Value: 0x0Fh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				EER_ADDR[11:8]			

Bit Number	Bit Mnemonic	Description
7-4	-	-
3-0	EER_ADDR[11:8]	EEP_ADDR[11:8] address setting, paired with EER_ADDR[7:0] to form a 12-bit address

-: unimplemented.

E²PROM Control Register EER_TCTL[3:0] (XFR: 0xE4) **Reset Value: 0x08h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	W	W	W	W	W	W
Name	Reserved	Reserved	EER_ERASE	EER_PROG	EER_TCTL[3:0]			

Bit Number	Bit Mnemonic	Description
7	Reserved	-
6	Reserved	-
5	EER_ERASE	1: E²PROM proceeds ERASE (256 Bytes)/page 0: Did not proceed ERASE
4	EER_PROG	1: E²PROM proceeds PROGRAM (1 Byte) 0: Did not proceed PROGRAM
3-0	EER_TCTL[3:0]	E²PROM ERASE/PROGRAM time setting **(see "Note")**

-: unimplemented.

E²PROM Data Register EER_DAT0[7:0] (XFR: 0xE8) **Reset Value: 0x00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	EER_DAT0[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	EER_DATA[7:0]	E²PROM Data Register

Note:

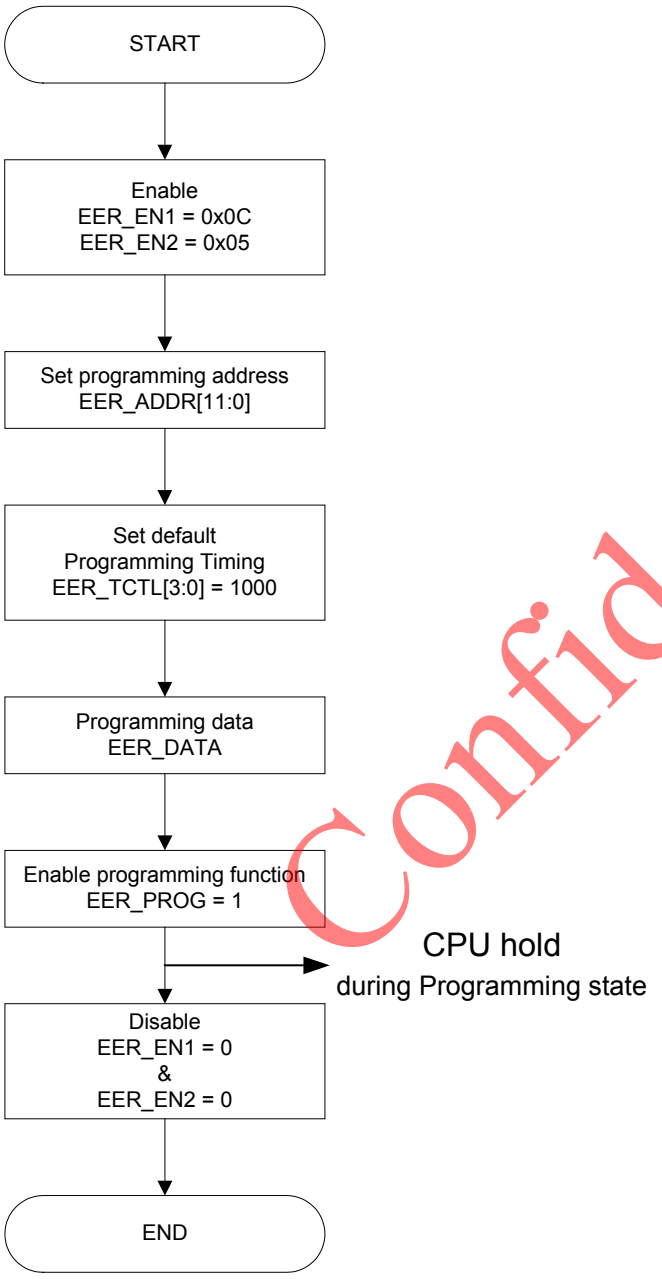
1. In programming, or erasing E²PROM function, all functions are halt state.
2. If MCU_CLK = 12 MHz
   Default: EER_TCTL[3:0] = 1000, so programming time = 28 μ sec ~ 32 μ sec
   and erasing time = 28 msec ~ 32 msec

E²PROM Clear Range and Address Setting (Cleared data 0xFF)

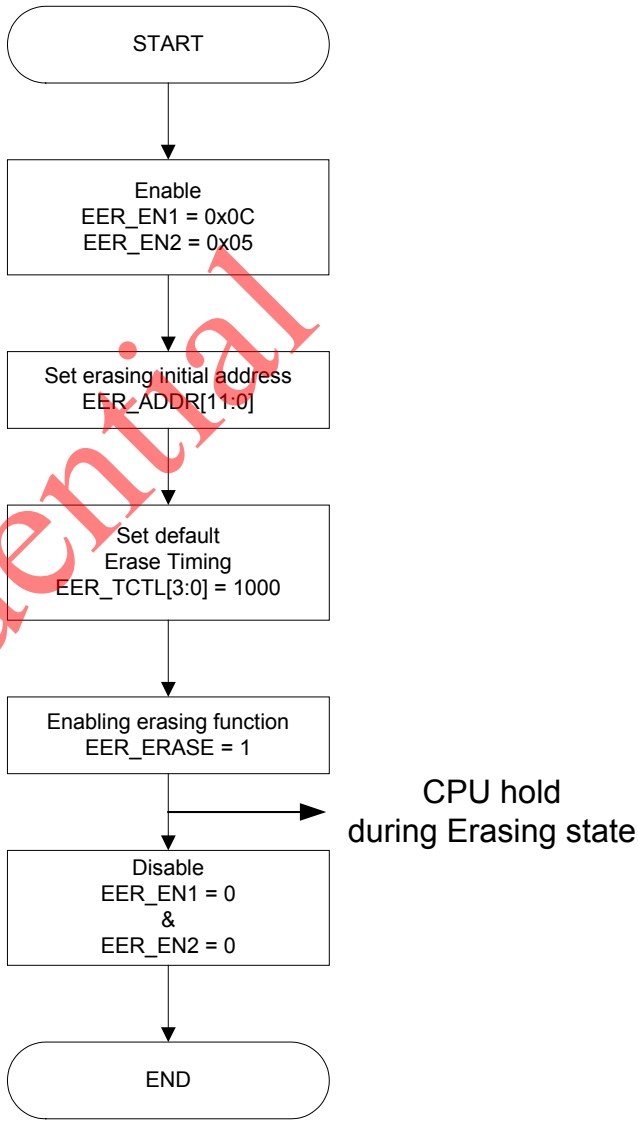
Flash address	EER_ADDR[11:8]	EER_ADDR[7:0]	Erase Range	Remark
0x3000	0000	0000 0000	0x3000 ~ 0x30FF	
0x3100	0001	0000 0000	0x3100 ~ 0x31FF	
0x3200	0010	0000 0000	0x3200 ~ 0x32FF	
0x3300	0011	0000 0000	0x3300 ~ 0x33FF	
0x3400	0100	0000 0000	0x3400 ~ 0x34FF	
0x3500	0101	0000 0000	0x3500 ~ 0x35FF	
0x3600	0110	0000 0000	0x3600 ~ 0x36FF	
0x3700	0111	0000 0000	0x3700 ~ 0x37FF	
0x3800	1000	0000 0000	0x3800 ~ 0x38FF	
0x3900	1001	0000 0000	0x3900 ~ 0x39FF	
0x3A00	1010	0000 0000	0x3A00 ~ 0x3AFF	
0x3B00	1011	0000 0000	0x3B00 ~ 0x3BFF	
0x3C00	1100	0000 0000	0x3C00 ~ 0x3CFF	
0x3D00	1101	0000 0000	0x3D00 ~ 0x3DFF	
0x3E00	1110	0000 0000	0x3E00 ~ 0x3EFF	

E²PROM Enable Flow chart:

Programming function:



Erasing function:



7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Min	Max	Units
D.C. Supply Voltage	-0.3	5.5	V
Input/Output Voltage	VSS -0.3	VDD +0.3	V
Ambient Temperature	-40	85	℃
Storage Temperature	-60	125	℃

7.2 Recommended Operating Ratings

Parameter	Symbol	Specification			Units
		Min	Typ.	Max	
Power Voltage	V_{DD}	2.0		5.5	V
Main Frequency	F_{main}		12		MHz
Operating Temperature	T_{OPR}	-40		85	℃

7.3 DC Electrical Characteristics (V_{DD} = 5V, -40℃ to +85℃)

Parameter	Symbol	Pin/condition	Specification			Units
			Min	Typ.	Max	
Schmitt Trigger from low to high (note 1)	V_{T+}		1.9		5.5	V
Schmitt Trigger from low to high (note 2)	V_{T+}		1.9		3.6	
Schmitt Trigger from high to low	V_{T-}				1.2	V
Output high voltage	V_{OH4mA} (note 3)	I_{OH} = 4mA	2.4			V
	V_{OH8mA} (note 4)	I_{OH} = 8mA	2.4			
Output low voltage	V_{OL4mA} (note 3)	I_{OL} = 4mA			0.4	V
	V_{OL8mA} (note 4)	I_{OL} = 8mA			0.4	
Input Leakage Current	I_{OZ}	V_O = 0V or 3.3V		±0.01	±1	μA
Pull-up Resistor	R_{PH}			50		KΩ
Normal Mode At 12 MHz	I_{VDD12M}	No load on output		4		mA
Normal Mode At 6 MHz	I_{VDD6M}	No load on output		2.5		mA
Normal Mode At 3 MHz	I_{VDD3M}	No load on output		1.5		mA
Normal Mode At 1 MHz	I_{VDD1M}	No load on output		1		mA
Idle Mode	I_{VDDS1}	No load on output		400		μA

Parameter	Symbol	Pin/condition	Specification			Units
			Min	Typ.	Max	
Sleep Mode	I_{VDDS2}	No load on output		100		μA
Power-saving Mode	I_{VDDS3}	No load on output		5		μA
RTC Mode	I_{VDDRTC}	No load on output		1		μA

Note 1: For GPIOA0~A6, GPIOC0~C7 and NRST pin, the biggest input voltage is +5.5v (= 5V+0.5V), and the biggest input voltage of GPIOC1 is +3.6V in UG320/32A package.

Note 2: For GPIOA7, GPIOB0~B7, and GPIOC1, the input maximum voltage of XTALI is +3.6V(=3.3V+0.3V).

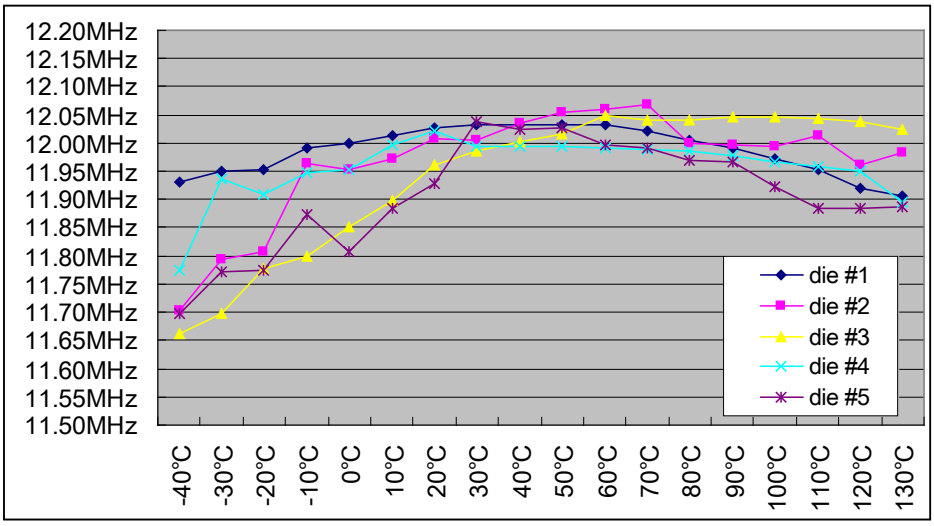
Note 3: Except GPIOA0, GPIOA3, GPIOA4 & GPIOC5, the sink/source current of the rest is 10mA.

Note 4: The maximum sink/source current of GPIOA0, GPIOA3, GPIOA4, and GPIOC5 is 20mA.

7.4 Internal 12 MHz RC Oscillator Accuracy table

Parameter	Symbol	Pin/condition	Specification			Units
			Min	Typ.	Max	
RC frequency	F_{RC}	VDD = 5V		12		MHz
Frequency tolerance @VDD5 = 5V (fixed)	$\Delta F_{RCH1}/F_{RCH}$	Without external oscillator for calibrating 25°C		±1		%
		0°C ~ 70°C		±2		%
		-40°C ~ 85°C		±3		%
Frequency tolerance @VDD5 = 5V (fixed)	$\Delta F_{RCH2}/F_{RCH}$	With external oscillator for calibrating -40°C ~ -85°C			±1	%

RC Oscillator Frequency vs. Temperature



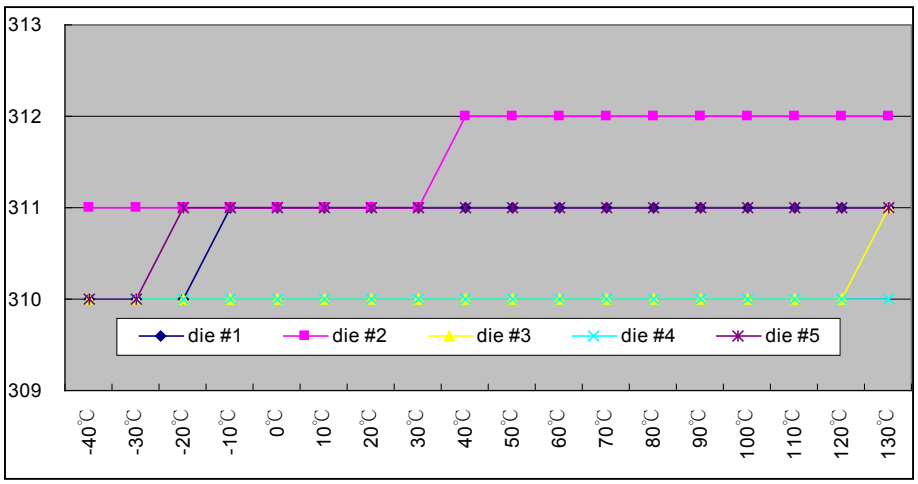
7.5 Internal Low Speed RC Oscillator

Parameter	Symbol	Pin/condition	Specification			Units
			Min	Typ.	Max	
RC frequency (@VDD5 = 5V)	F_{RCL}		110	128	145	kHz
	$\Delta F_{RCL}/F_{RCL}$	Without external oscillator for calibrating -40°C ~ -85°C			±5	5%

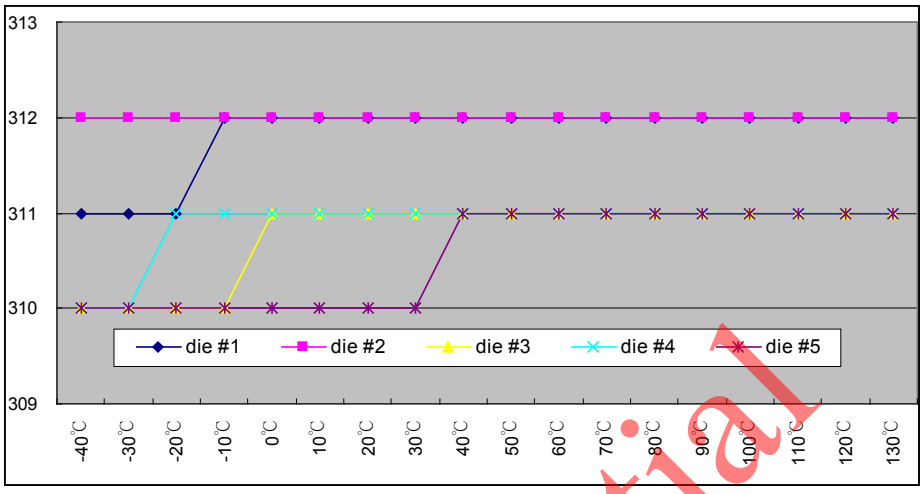
7.6 A/D Converting Characteristics

Parameter	Symbol	Pin/condition	Specification			Units
			Min	Typ.	Max	
Resolution					10	bit
Absolute Accuracy	E_{IL}	AREF = 3.3V			±2	LSB
Relative Accuracy	E_{DL}	AREF = 3.3V			±1	LSB
Compensation Accuracy	E_{OFS}	AREF = 3.3V			±1	LSB
Amplified Accuracy	E_{GAN}	AREF = 3.3V			±3	LSB
Analog Input Voltage Range	V_{AN}	VDD5 = 5V	VSS		CAP33 (AREF)	V
		VDD33 = 3.3V	VSS		VDD33 (AREF)	V
Analog Reference Voltage	V_{REF}		2		CAP33 (VDD33)	V
Converting Time	T_{CT}		16			μs
ADC power consumption	IADC1	VDD33 = 3.3V		600		μA

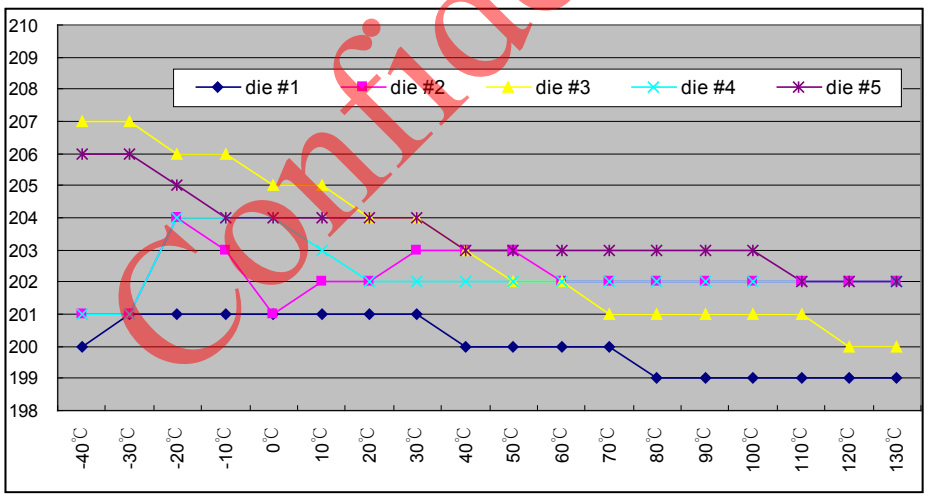
(a) AD Converting data vs. Temperature, when V_{AN} input = 1V at "ADC VREF voltage = CAP33/VDD33 power = 3.3V"



(b) AD Converting data vs. Temperature, when V_{AN} input = 1V at "ADC VREF voltage = AREF pin = 3.3V"



(c) AD Converting data vs. Temperature, when V_{AN} input = 1V at "VREF voltage = internal bandgap voltage"

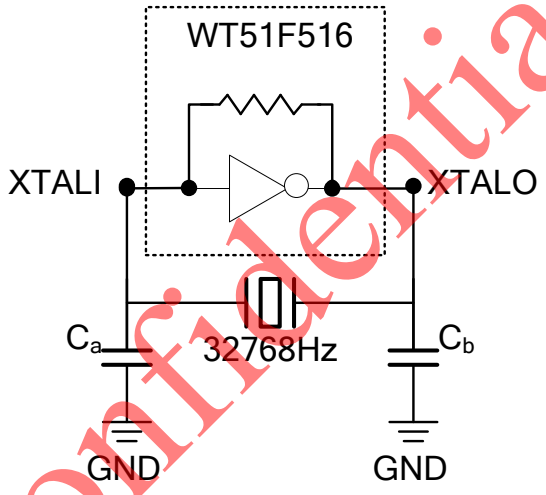


7.7 Crystal Oscillator

Parameter	Symbol	Pin/condition	Specification		
			Min	Typ.	Max
Frequency range	F_O			32.768	
External capacitance(1)	C_a/C_b		10		68

Notes:

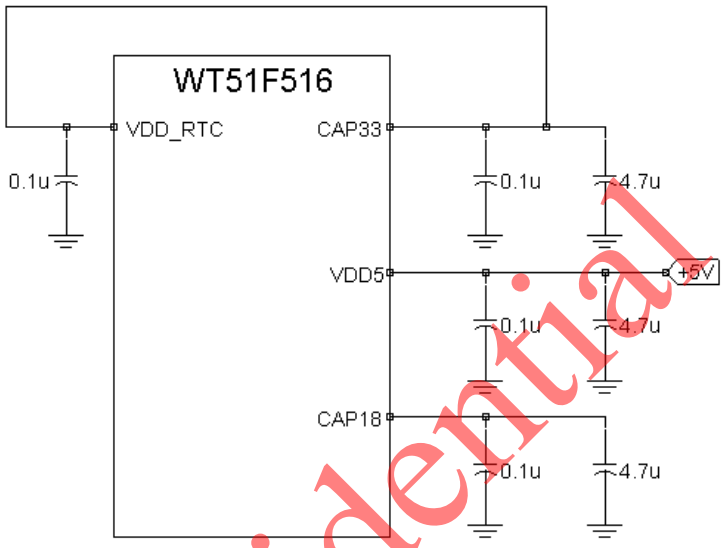
1. **Crystal load capacitance $C_L = \frac{Ca*Cb}{(Ca+Cb)} + Cs$ (C_S is stray capacitances and Crystal load capacitance value to look for in the data sheet of the crystal is C_L). The recommended capacitor value (C_a and C_b) are in the range 10-68pF.**



8. Application Circuits

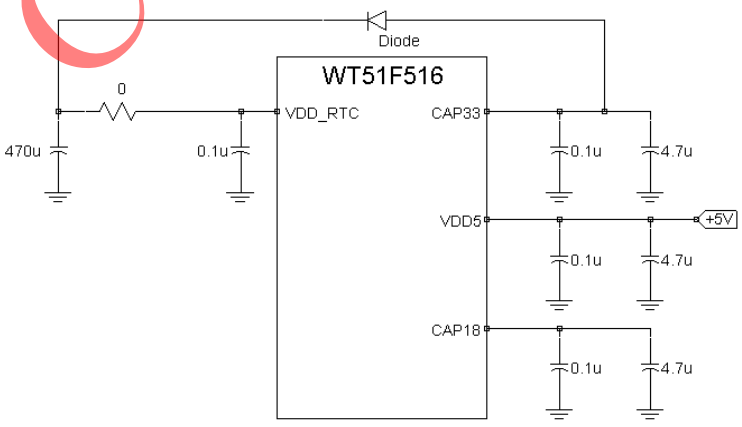
8.1 +5.0V power Supply

For 51F516-RG480WT/51F516-UG320/32AWT



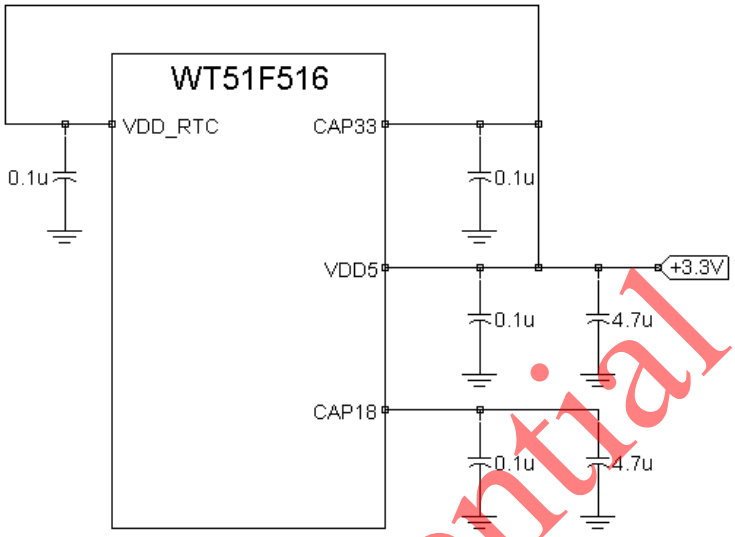
For 51F516-RG480WT/51F516-UG480WT

RTC external super-cap or battery reference circuit

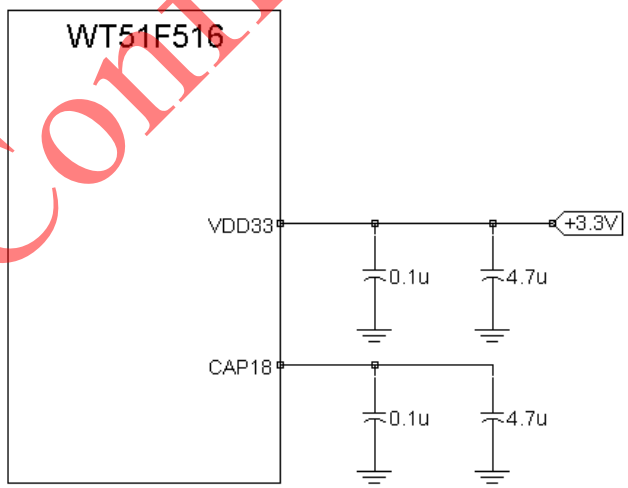


8.2 +3.3V power Supply

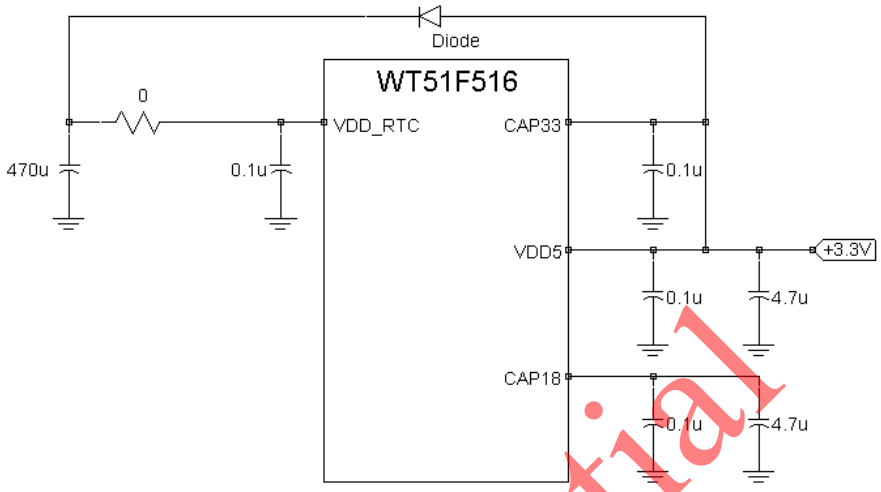
For 51F516-RG480WT/51F516-UG320/32AWT



For 51F516-OG200WT/51F516-SG161WT

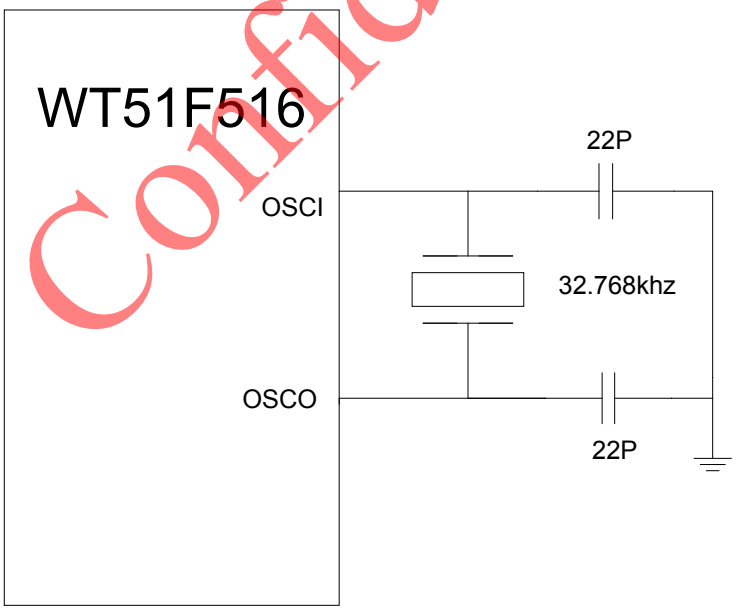


For 51F516-RG480WT/51F516-UG320/32AWT



8.3 Oscillator Circuits

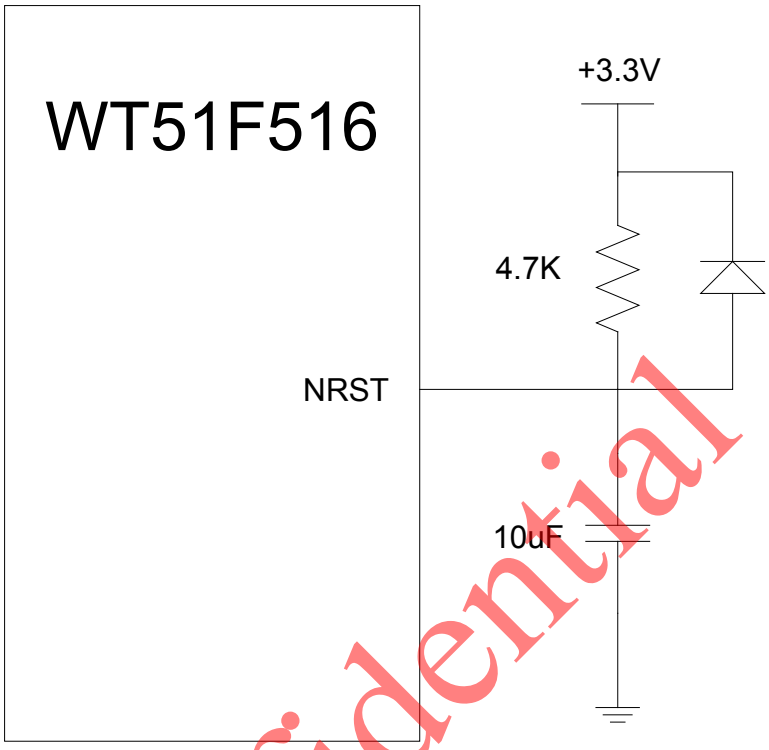
8.3.1 External 32.768 kHz Crystal Oscillator



Note: WT51F516 has built-in internal RC oscillators, thus external crystal oscillators are not essential. If for more precise application, external crystal oscillator is available for use.

* Crystal load capacitance $C_L = \frac{Ca * Cb}{(Ca + Cb)} + Cs$ (C_S is stray capacitances and Crystal load capacitance value to look for in the data sheet of the crystal is C_L.)

8.4 RESET Circuit



9. Product Naming Rule

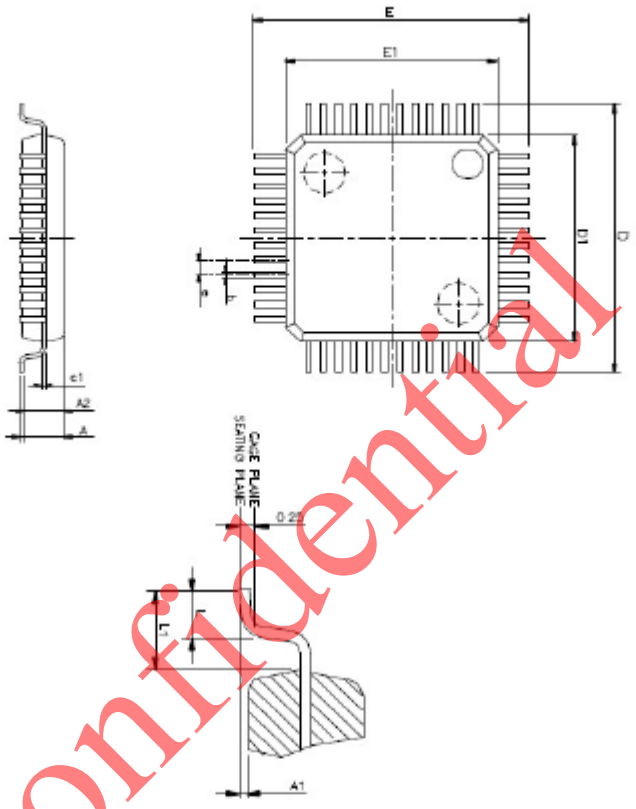
WT	Consumption market	LCD function	Seed code (Family)	Flash Size (K Bytes)		Remarks
WT	5	1F	1	0	4	5: MCU/DSP embedded, used in general-purpose or consumption market related product. 1X: 8-bit MCU 1F: Flash type 8-bit MCU without LCD function
			5	1	6	
WT	5	6F	1	0	8	5: MCU/DSP embedded, used in general-purpose or consumption market related product. 6X: LCD back light module controller 6F: Flash type 8-bit MCU with LCD function
			2	1	6	

10. Ordering Information

Package Type	Package Outline	Part Number
LQFP48	7mm x 7mm	WT51F516-RG480WT
QFN32	5mm x 5mm	WT51F516-UG320WT
QFN32	5mm x 5mm	WT51F516-UG32AWT
SSOP20	150 mil	WT51F516-OG200WT
SOP16	150 mil	WT51F516-SG161WT
DIE	-	WT51F516-HXXXWT

11. Package Dimension

11.1 48-Pin LQFP

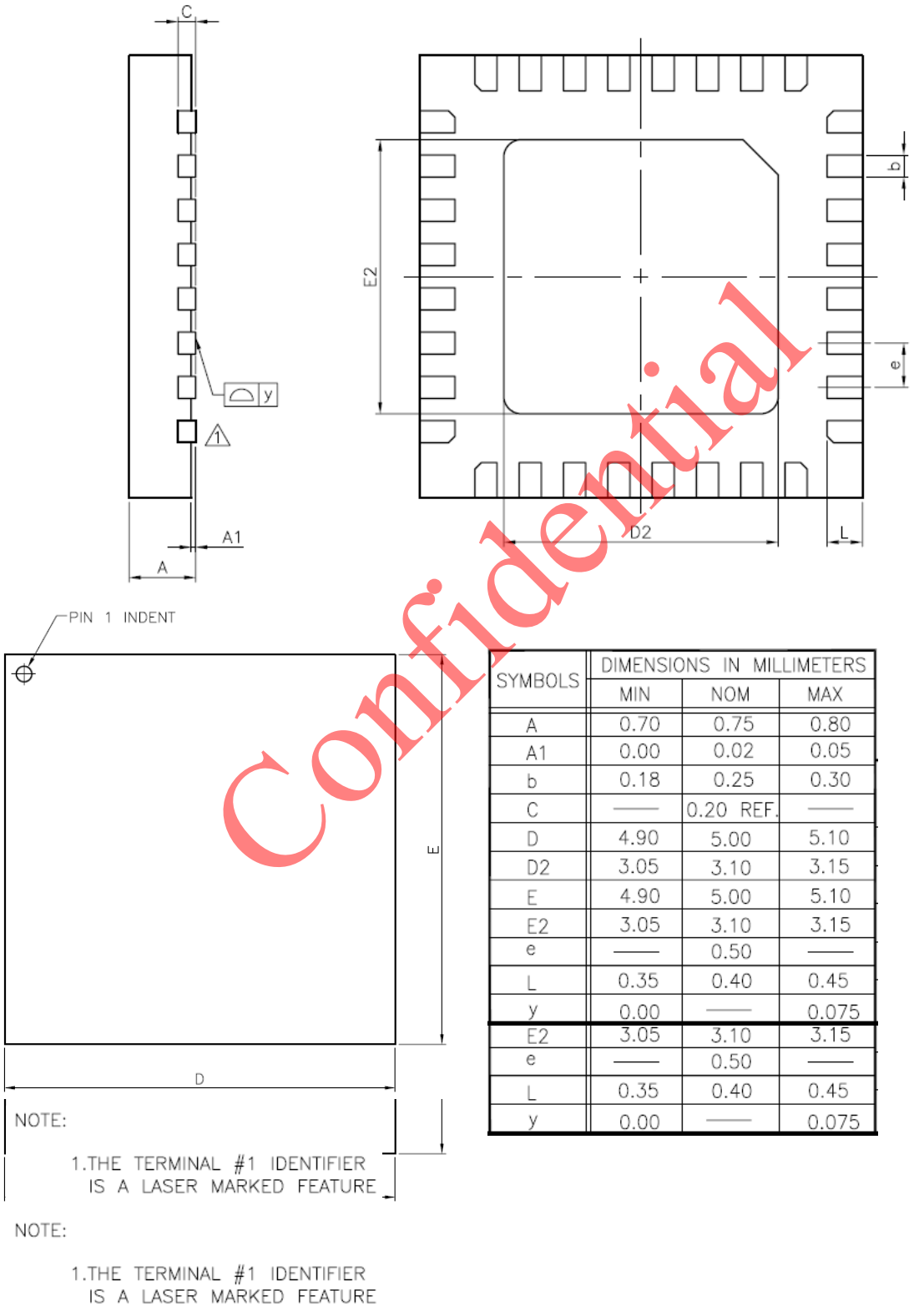


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

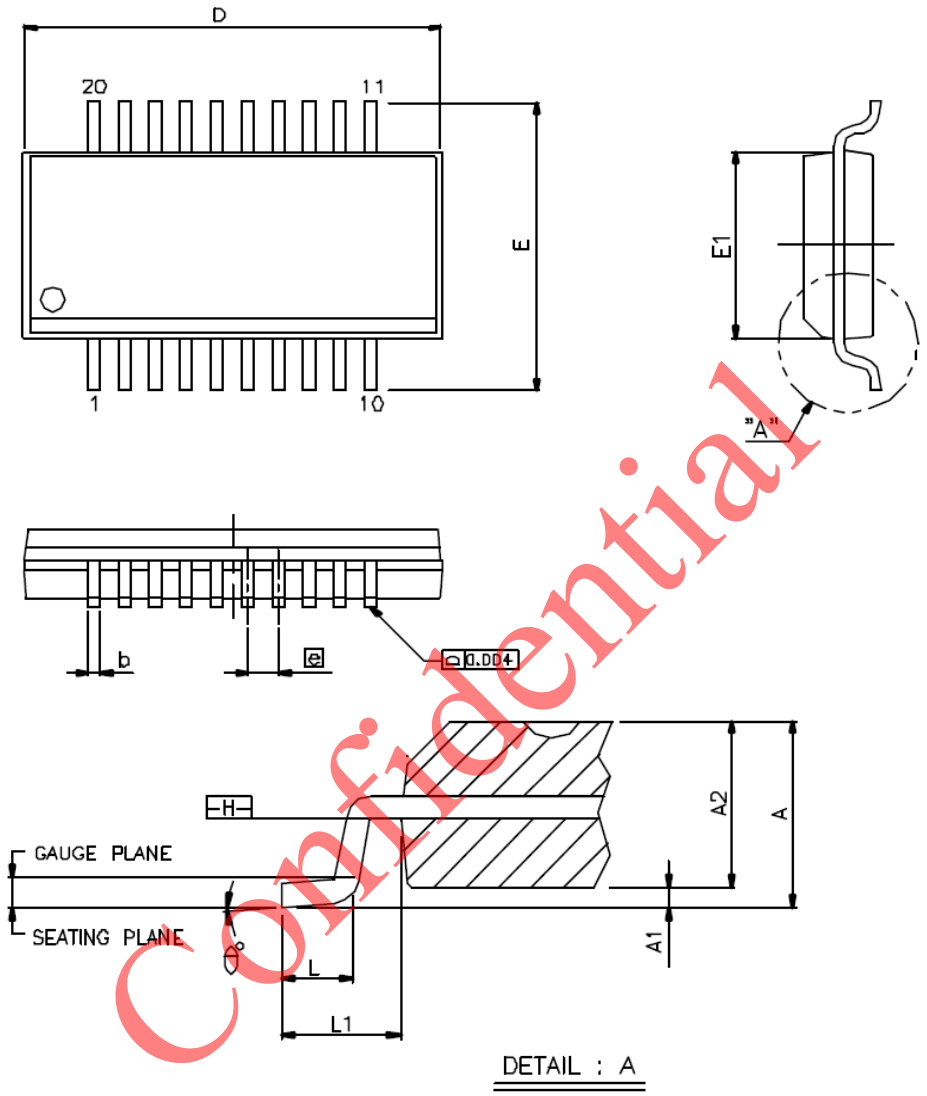
NOTES:
1.JEDEC OUTLINE:MS-026 BBC
2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

11.2 QFN32



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
C	——	0.20 REF.	——
D	4.90	5.00	5.10
D2	3.05	3.10	3.15
E	4.90	5.00	5.10
E2	3.05	3.10	3.15
e	——	0.50	——
L	0.35	0.40	0.45
y	0.00	——	0.075
E2	3.05	3.10	3.15
e	——	0.50	——
L	0.35	0.40	0.45
y	0.00	——	0.075

11.3 SSOP20

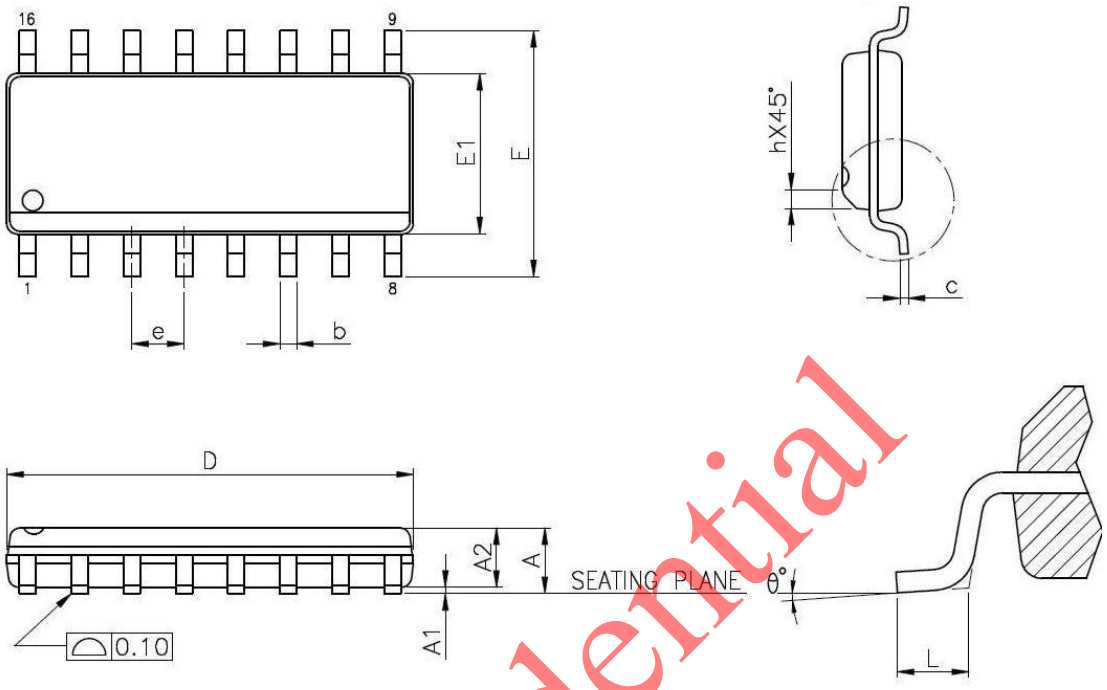


SYMBOLS	MIN.	NOM.	MAX.
A	0.053	0.064	0.069
A1	0.004	0.006	0.010
A2	–	–	0.059
b	0.008	–	0.012
C	0.007	–	0.010
D	0.337	0.341	0.344
E	0.228	0.236	0.244
E1	0.150	0.154	0.157
e	0.025 BASIC		
L	0.016	0.025	0.050
L1	0.041 BASIC		
θ°	0°	–	8°

UNIT : INCH

NOTES:
1. JEDEC OUTLINE : MO-137 AD
2. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006" PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD MOLD PROTRUSIONS. INTERLEAD MOLD PROTRUSIONS SHALL NOT EXCEED 0.010" PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.004" TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.002" AT LEAST

11.4 SOP16



SYMBOLS	STANDARD	
	MIN.	MAX.
A	-	1.75
A1	0.10	0.25
A2	1.25	-
b	0.31	0.51
c	0.10	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.50
θ°	0	8

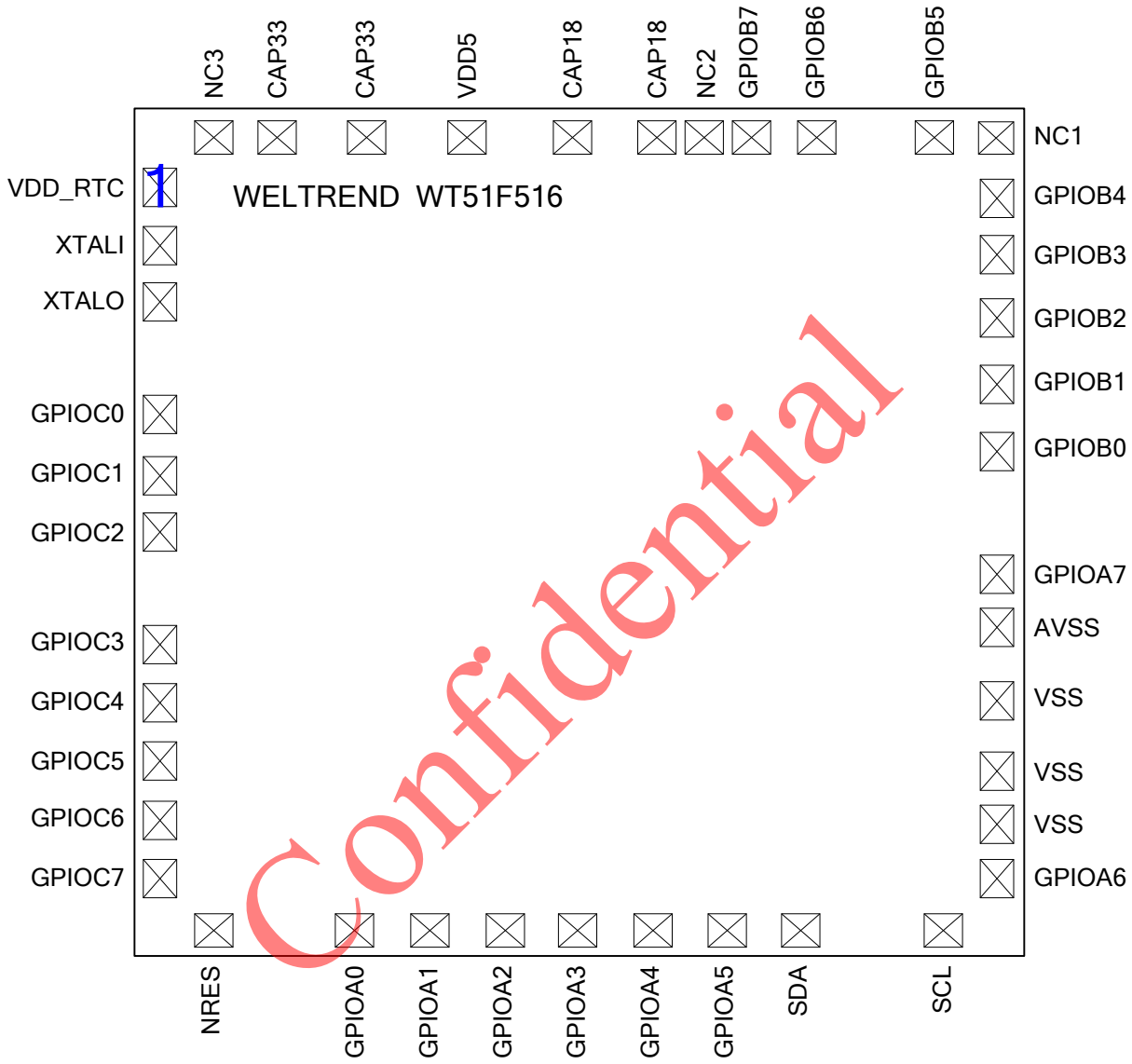
UNIT: mm

NOTES:

1. JEDEC OUTLINE:
   MS-012 AC REV.F (STANDARD)
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm. PER SIDE

DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE

11.5 Pad Diagram



Location Table

No	Name	X	Y	*	No	Name	X	Y	*
1	VDD_RTC	46.18	1606.82	A	22	VSS	1803.82	268.53	A
2	XTALI	46.18	1487.12	A	23	VSS	1803.82	376.88	A
3	XTALO	46.18	1367.42	A	24	VSS	1803.82	528.05	A
4	GPIOC0	46.18	1129.69	A	25	AVSS	1803.82	681.95	A
5	GPIOC1	46.18	1006.99	A	26	GPIOA7	1803.82	795.61	A
6	GPIOC2	46.18	884.29	A	27	GPIOB0	1803.82	1055.415	A
7	GPIOC3	46.18	645.71	A	28	GPIOB1	1803.82	1192.735	A
8	GPIOC4	46.18	523.01	A	29	GPIOB2	1803.82	1330.055	A
9	GPIOC5	46.18	400.31	A	30	GPIOB3	1803.82	1467.375	A
10	GPIOC6	46.18	277.61	A	31	GPIOB4	1803.82	1587.185	A
11	GPIOC7	46.18	154.91	A	32	NC1	1805.32	1713.82	C
12	NRES	154.45	46.18	B	33	GPIOB5	1677.62	1713.82	B
13	GPIOA0	458.43	46.18	B	34	GPIOB6	1425.81	1713.82	B
14	GPIOA1	613.83	46.18	B	35	GPIOB7	1286.53	1713.82	B
15	GPIOA2	769.23	46.18	B	36	NC2	1188.79	1713.82	B
16	GPIOA3	924.63	46.18	B	37	CAP18	1091.79	1713.82	B
17	GPIOA4	1080.03	46.18	B	38	CAP18	913.595	1713.82	B
18	GPIOA5	1235.43	46.18	B	39	VDD5	696.225	1713.82	B
19	SDA	1390.83	46.18	B	40	CAP33	478.87	1713.82	B
20	SCL	1695.55	46.18	B	41	CAP33	291.68	1713.82	B
21	GPIOA6	1803.82	154.45	A	42	NC3	153.18	1713.82	B

Note 1: The origin of pad location shown here is at lower-left corner of die.

*Note 2: *PAD Window.*

A: 66um x 73um

B: 73um x 66um

C: 63um x 66um

Note 3: To stabilize the supply voltages, please connect 0.1uF and 4.7uF bypass capacitors between CAP18/ CAP33/VDD5/VDD_RTC and VSS.

Note 4: NC1,NC2,NC3 pin no connection for normal application.

Note 5: All VSS pin need connect together. (No: 22, 23, 24, 25)

Note 6: All CAP18 pin need connect together. (No: 37, 38)

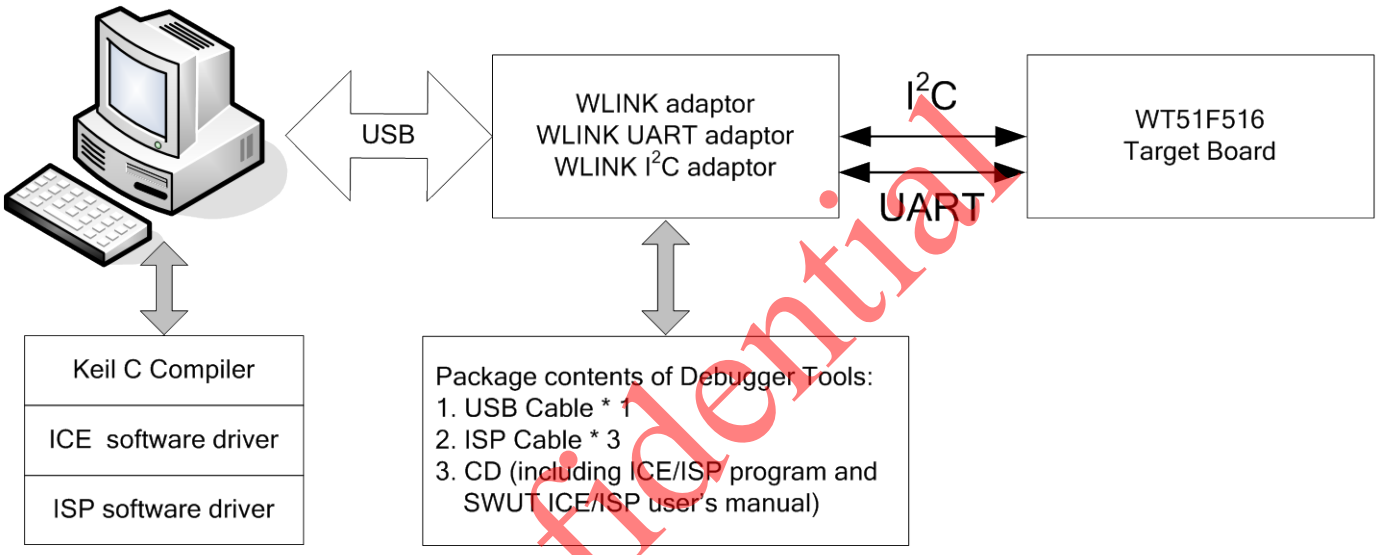
Note 7: All CAP33 pin need connect together. (No: 40, 41)

Note 8: VDD_RTC pin may be connect with CAP33, except it has its own power source.

12. Development Tools

WT51F516 can work together with Keil C51 development environment. WLINK adaptor can link PC and WT51F516 evaluation board via ICE/ISP driver, and the debugger tools, demo board application software can perform In-Circuit Emulator (ICE) and In-system Programming (ISP) in Windows Win98/2000/XP/Win7.

The development kits are illustrated in the figure below:



Note: Refer to ICE/ISP user's manual and WLINK Application Notes for more details.

13. Revision History

Version	History	Date
1.1	Initial issue	Apr. 2012
1.11	Features add QFN32, SSOP20, and SOP16 descriptions	July 2013
1.12	Add UG32A package	Mrach 2015